

7. Lotspeich, Electrooptic Light-Beam Deflection, IEEE Spectrum, February 1968.
8. Harris, Digital Laser Beam Deflection, Laser Focus, April 1967.
9. Myers, The Electron Beam Scanlaser, IBM Journal of Research and Developemnt, September 1967.
10. Kulcke, et al, Digital Light Deflectors, Applied Optics, October 1966.

**NAVAL TRAINING DEVICE CENTER
TRAINING DEVICE COMPUTER SYSTEM
(TRADEC)**

F. R. COOPER
Computer Laboratory
Naval Training Device Center

The purpose of this presentation is to apprise industry of the computational facility to be installed at NTDC - hereafter to be referred to as the TRADEC system. TRADEC is the abbreviation for training Device Computer.

I will indicate the organizational structure under which the TRADEC installation will operate. I will review the purpose, present status and characteristics of the installation itself.

The TRADEC facility is under the jurisdiction of the Research Directorate, Code 50. Reporting to the Associate Technical Director are five research laboratories, one of which is the Computer Laboratory, Code 54. The direct responsibility for the operation of subject facility rests with Code 54. The Computer Laboratory is headed by Mr. Milton Fischer.

On 28 June 1967 a contract was awarded to Sylvania Electronic Systems, East Division, Needham, Mass., to provide a modern simulation and computation facility to meet the needs of the Center's research programs for a number of years. This contract culminates in the delivery of the system in March 1969, and in its becoming operational the second quarter of 1969.

The TRADEC system, along with existing equipment, will be used in the conduct of research in simulation, and will provide support for the Center's various projects. It will be utilized in all phases of our simulation research program.

Figure 36 is an artist's concept of the physical plant, presently under construction, which will house the TRADEC system and existing equipment. The site consists of an existing building to which a new wing is being attached. The existing building has been modified and will accommodate the new digital and the existing analog computer systems. The new attached wing will house the motion and cockpit systems.

The TRADEC digital computer is a Scientific Data Systems Sigma 7. Figure 37 is a scene of the computer at Sylvania where system integration is in process.

The digital hardware system: A simplified block diagram of the digital computer is shown in Figure 38. Direct access to memory is available to the central processing unit, peripheral I/O processors, and a special interface I/O processor.

A description of each of these areas will clearly indicate the hardware and the capability of the digital system.

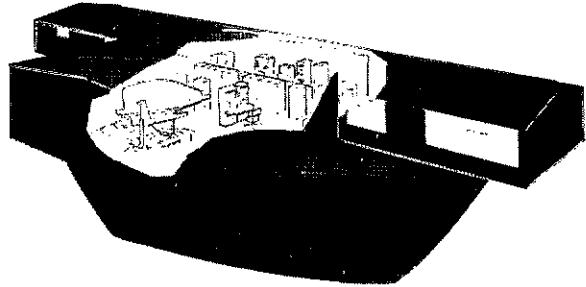


Figure 36. Artist's Concept of the Physical Plant



Figure 37. Sigma 7 Installation

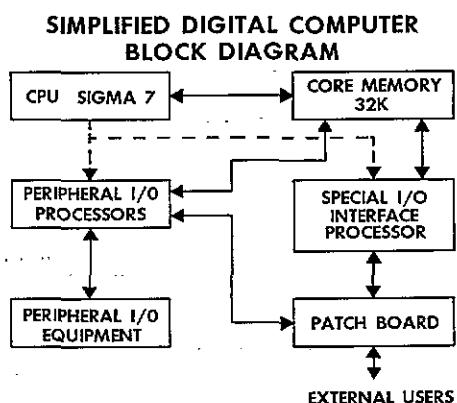


Figure 38.

SIGMA 7 MEMORY AND CENTRAL PROCESSOR CHARACTERISTICS

32 BIT WORD SIZE

32,768 WORDS OF CORE MEMORY

850 NSEC. MEMORY CYCLE TIME

1.8 USEC. FULL WORD ADD

4.9 USEC. FULL WORD MULTIPLY

12.7 USEC. FULL WORD DIVIDE

Figure 39.

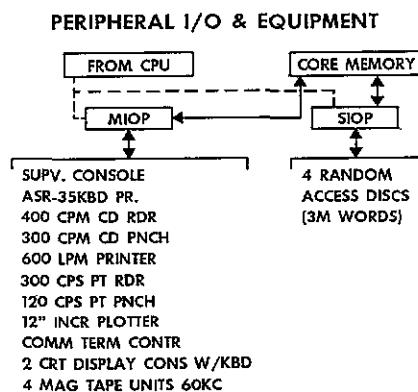


Figure 40.

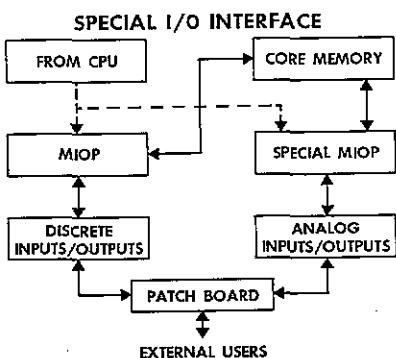


Figure 41.

Memory and CPU characteristics are given in Figure 39. The Sigma 7 is a 32 bit word machine. Core storage, at the present time, has a capacity of 32,768 words. The memory cycle time is 850ns. A full word add operation is accomplished in 1.8 usec, full word multiply in 4.9 usec, and a full word divide in 12.7 usec. Peripheral devices are controlled by I/O processors which, after being initiated by the central processor, carry out input/output instructions independently (see Figure 40). The list of available peripheral equipment includes:

- 1 - System Supervisory Console
- 1 - 400 cpm Card Reader
- 1 - 300 cpm Card Punch
- 1 - 600 lpm Printer
- 1 - 300 cps Paper Tape Reader
- 1 - 120 cps Paper Tape Punch
- 1 - ASR-35 Keyboard Printer
- 4 - 60KC - Magnetic Tape Drives (9 track)
- 1 - 12" Calcomp Incremental Plotter
- 4 - Communication Terminals, Provision for
- 2 - CRT Display Consoles w/Keyboard Inputs
- 4 - Random Access Discs with 3 million word capacity and 17ms access time is controlled by a separate I/O processor.

The special I/O interface (Figure 41) provides access to, and control by, the TRADEC system. This interface is made available to all external users of the digital system through a patch board. This special interface consists of 240 discrete inputs, 240 discrete outputs, 32 analog inputs, and 96 analog outputs.

The digital computer interfaces with all other elements of the TRADEC system through this patch board -- for example the motion system, F4E cockpit, the existing REAC 550 analog computer, and others.

TRADEC will have the following software systems (Figure 42):

Assemblers: Symbol - (Includes symbol, procedures, lists; operates under Batch Processor Monitor, BPM.)

Meta-Symbol - (Operates under Stand Alone, or the Basic Control Monitor, BCM)

Compilers: Fortran IV - (Operates under the BPM)

Fortran IV-H - (Operated under the BCM)

Monitors: Basic Control Monitor

Batch Time Sharing Monitor

Others: F4E Simulator Program

Stand Alone Systems

Standard SDS Diagnostics

Math Library

Sort/Merge

1401 Simulator

MANAGE (A Management Information System)

In general, users of the TRADEC facility will be required to furnish their own programs in a form directly readable by the facility peripheral equipment. A standards manual is being prepared for the TRADEC installation and will be published in the near future.

TRADEC SOFTWARE SYSTEMS

ASSEMBLER	COMPILER
SYMBOL	FORTRAN IV
META-SYMBOL	FORTRAN IV-H

MONITOR

BCM-BASIC CONTROL
BPM-BATCH PROCESSOR
BTM-BATCH TIME SHARING

OTHER

F4E SIMULATOR
STAND ALONE SYSTEMS
STND. DIAGNOSTICS
MATH LIBRARY

Figure 42.

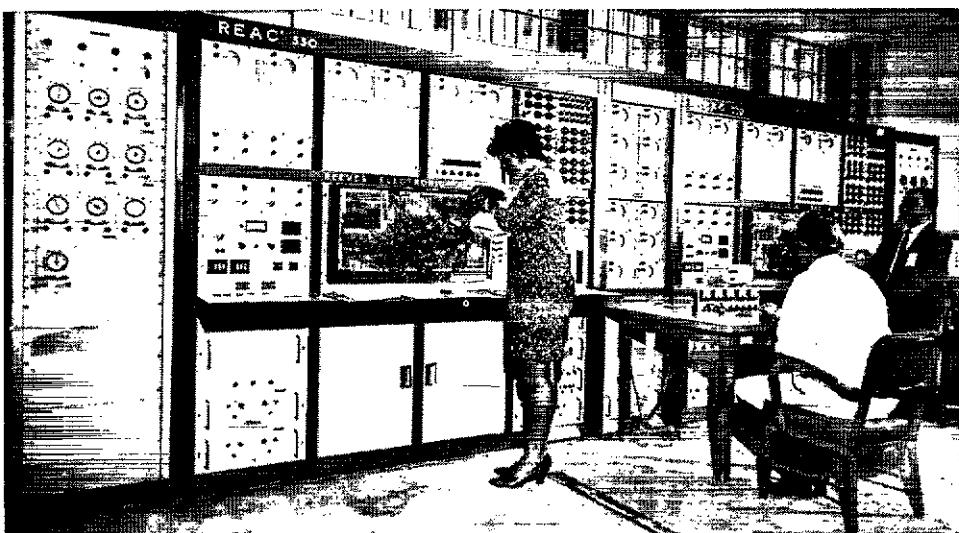


Figure 43. REAC 550 Photograph

ANALOG COMPUTER

REAC 550

200 OPERATIONAL AMPLIFIERS

24 SERVOS

PERIPHERAL EQUIPMENT

X-Y PLOTTER

BRUSH RECORDER

PRINTER

Figure 44. REAC 550 Computer Characteristics

The Computer Laboratory currently has in operation a REAC 550 analog computer shown in Figure 43. Figure 44 indicates a partial list of the analog system hardware.

The REAC 550 is capable of high speed repetitive and iterative operation. The REAC's internal clock permits automatic reset and operate periods as short as one msec. Provisions are being made for timing and control of the analog computer by the digital computer through the patch board, forming a substantial hybrid capability. This hybrid interface will be controlled by the special I/O interface previously described. Under consideration is automatic setting of the REAC's potentiometers by the Sigma 7.

The TRADEC motion system, shown in Figure 45, was designed and constructed by Canadian Aviation Electronics, Ltd., Montreal, Canada, subcontractor to Sylvania. The motion system provides four degrees of freedom with the characteristics given in Figure 46.

The simulation cockpit, shown in Figure 47, was designed by Sylvania. The cockpit design permits a tandem, or side-by-side, seating arrangement. The simulator program being supplied by Sylvania is for an F4E aircraft. The seating arrangement, therefore, is in tandem and the panels and controls are those of an F4E.

In conclusion, I have, in the time allowed, described the new computational facility to be installed in March 1969 at NTDC, which is dedicated to research in all aspects of simulation training.

It has been a privilege to have introduced the TRADEC system and we look forward to working with Industry in the future in advancing the state-of-the-art of simulation for training.



Figure 45. Motion System Photograph

TRADEC MOTION SYSTEM CHARACTERISTICS.

	LEFT (UP)	RIGHT (DOWN)
ROLL	MAX. 16.0°	16.2°
	ACCEL. 46°/SEC ²	52°/SEC ²
PITCH	MAX. 21.5°	11.5°
	ACCEL. 24.7°/SEC ²	17.9°/SEC ²
HEAVE	MAX. 25.4"	-
	ACCEL. 22.0"/SEC ²	-
YAW	MAX. 18.0°	19.5°
	ACCEL. 22.6°/SEC ²	22.6°/SEC ²
MAX. WEIGHT CAPACITY-10,000 LBS.		

Figure 46.

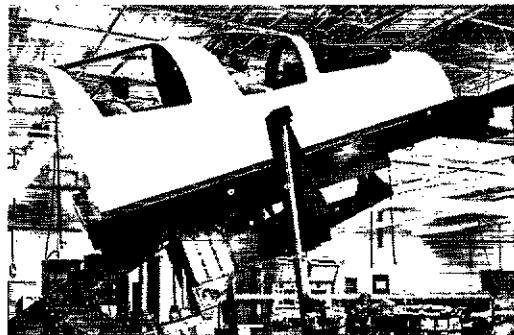


Figure 47. Cockpit and Motion System