ANALYSIS OF FIDELITY REQUIREMENTS

FOR SIMULATED ELECTRONIC MAINTENANCE TRAINING EQUIPMENT

Dr. L. Bruce McDonald
Grace P. Waldrop

McDonald & Associates, Inc.
988 Woodcock Rd., Orlando, FL. 32803

Dr. Richard Reynolds

Human Factors Laboratory, Naval Training Equipment Center
Orlando, FL. 32813

ABSTRACT

Maintenance training simulators have proven to afford equal or superior training at a lower life cycle cost than actual equipment trainers when teaching troubleshooting based on front panel indications, failure symptoms and some in-drawer visual indicators. The purpose of the study was to determine the effects of two-dimensional and three-dimensional fidelity of simulation and three levels of reduced accessibility to test points during training, on student troubleshooting performance while locating faults at the component level. A total of 186 students were observed and tested in the ET Splice modules of a Navy Basic Electricity and Electronics course. Conclusions are drawn about the relative training effectiveness of simulated and actual boards and recommendations are made in selecting active test points on simulated printed circuit boards.

INTRODUCTION

Over the last few years, computer simulation maintenance trainers have made significant inroads against actual equipment trainers (AET's) in hands-on electronic maintenance training. Simulators have proven to provide equal or superior training at a lower life cycle cost when teaching troubleshooting based on front panel indications, failure symptoms and some in-drawer visual indicators.

However, in the area of hands-on troubleshooting to the component level, the relative cost-effectiveness of AET's versus simulation trainers is not clearly understood. Actual equipment trainers are a higher fidelity simulation of the field equipment and theoretically should provide better transfer of training. However, high AET purchase costs and lower reliability leads to high life cycle costs. Trainers generally have a lower life cycle cost, but these savings are accompanied by a reduced fidelity of simulation; especially a reduced number of test points. Simulation engineers indicate that if all test points on a circuit board (50-100 points) are simulated, the complexity of modeling the correct test equipment readings for each failure at every point becomes prohibitive.

Another difference between AET's and simulation trainers is that trainers may utilize a photograph of a circuit board with test points available in appropriate locations. The training effects of this reduced fidelity of simulation have not yet been determined.

The general assumption is that AET is more costly and effective in training for troubleshooting to the component level, while simulation trainers are less expensive and less effective due to the limited number of test points and reduced visual fidelity. The question is which one is more cost-effective. Engineers can estimate the cost of a trainer for various numbers of simulated test points and visual representation based on previous experience. The question remains as to the relative effectiveness of a trainer depending on the fidelity of simulation and number of test points simulated. The purpose of this study was to determine the transfer of training to actual equipment derived from training on modified printed circuit boards with varying numbers of simulated test points represented photographically and in three dimensions.

METHOD

Initial Data Acquisition

Initial data were collected to determine the points most frequently probed by Basic Electricity and Electronics (BE&E) students. These initial data were required in order to select the points to be exposed during the experimental phase of the study.

Students were categorized as high, medium and low proficiency levels based on prerequisite course completion time. Trainees were observed during normal coursework and troubleshooting lessons. No changes were made in the current curriculum except for the additional troubleshooting session at the researcher's table. The observation of troubleshooting behavior resulted in the following data:

1) number of trainees probing each test point

2) sequential order of probes.

Apparatus

Subjects in the experimental study were tested using modified actual equipment in order to eliminate the expense of creating a software package to control specialized hardware. Printed circuit boards normally used in the trainer were modified to control access to test points. This modification was based on test points probed during the initial data acquisition.

Potential test points were created by soldering a short copper wire to the test point. Then the boards were sprayed with clear varnish to place an insulating coat over the entire board. Test points were made accessible by cutting away the coating on the end of the wire. By cutting away the varnish on different numbers of potential test points, experimental groups of test subjects were trained with varying numbers of accessible test points for hands-on practice. The test points made accessible matched those probed by 33%, 67% and 100% of the trainees in the initial data gathering phase. The board modification in Figure 1 simulates the effect of varying numbers of accessible test points on a high fidelity, three-dimension simulation of a PC board.

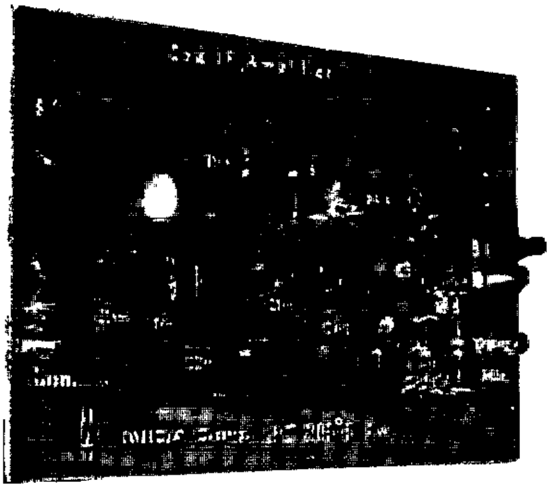

Figure 1 Three-Dimensional Simulation

Figure 2 Two-Dimensional Simulation

The board modification in Figure 2 simulates the effect of varying numbers of test points on a photographic simulation of a PC board. A photograph of the PC board was mounted over the actual board. Test points were created by placing a hole in the photograph, projecting the copper wire through, and coating it with varnish. Test points were then made accessible by cutting away the coating in the same manner as above.

Table 1 indicates the number of test points made accessible on the FM Radio Second IF Amplifier Board. Faults were grouped together such that the required minimum probe points would have a 90% overlap. The ratio between accessible points and the minimum number of points required was 4.50:1 for 100% accessibility, 2.75:1 for 67% accessibility, and 1.60:1 for 33% accessibility.

Table 1

Test Point Accessibility
FM 2nd/IF Amplifier Board

Fault Group	Fault	Minimum Tests Required*	Test Points Accessible 100%	67%	33%
1	Diode Open, Resistor Open	7	42	22	12
2	Resistor Open, Resistor Open	11	42	28	17
3	Transistor Short, Open Run	11	41	28	17

*NOTE: Using Half-Split Technique

Subjects

Test subjects were trainees in the ET Splice modules of a Navy BE&E course. A total of 186 trainees were included in data collection.

Experimental Design

A two-way analysis of variance design (see Figure 3) was used for the main independent variables of fidelity (actual boards vs photographic boards) and three levels of test point availability (100%, 67%, 33%), with a control group (unmodified boards).

Three different circuit boards were utilized in the study; an FM Radio First IF Amplifier board, FM Radio Second IF Amplifier board and a Power Supply board. Each had three fault group types. Trainee proficiency levels were matched for each treatment condition. The dependent variables were number of test points probed, time to probe, and number of trips to the learning supervisor before fault localization. In addition to the main experimental effects, the troubleshooting logic used by trainees was examined. The logic was examined for differences by experimental treatment, as well as analysis of what types of strategies were used most consistently and effectively.

		Fidelity	
		Three Dimensional	Two Dimensional
Test Points Exposed	100%	*	
	67%		
	33%		
	Contr.		

*Each cell balanced with 3 levels of proficiency and 3 fault groups.

Figure 3 Experimental Design

Procedures

When the subject trainees were ready for a practice session on one of the boards used in the study, they were assigned to the research station. The experimenter gave the trainee a pre-faulted board modified to one of the seven treatment conditions. Subjects proceeded to troubleshoot the board and take their exercise sheets to the school's learning supervisor for grading. This step was repeated with an identical board and treatment condition, but a different fault. When the learning supervisor determined the subject had mastered the board, the trainee was given an unmodified board to troubleshoot. This test was the criterion performance to measure transfer of training to actual equipment after practice on modified boards.

During the troubleshooting of both modified and unmodified boards, the experimenter recorded: the number of probes, probing time, subject comments and all other applicable data. These data were then analyzed to determine the training effects of simulation fidelity and test point availability on troubleshooting behavior using actual equipment.

RESULTS

Probes and Time

At the time this paper was prepared, analyses were completed for the FM Radio Second IF Amplifier board only. Results for the other boards will be reported at a later date.

The primary measures of effectiveness were number of probes and time required to locate the fault. Figure 4 exhibits the effects of percent points available, fidelity and student proficiency level on these two measures during criterion tests on actual equipment.

Students tended to probe fewer times and locate the fault in less time when trained on the board with 67% of the points accessible. However, this difference was not statistically significant. Students tended to probe fewer times and locate the fault in less time when trained on unmodified boards as opposed to 2D

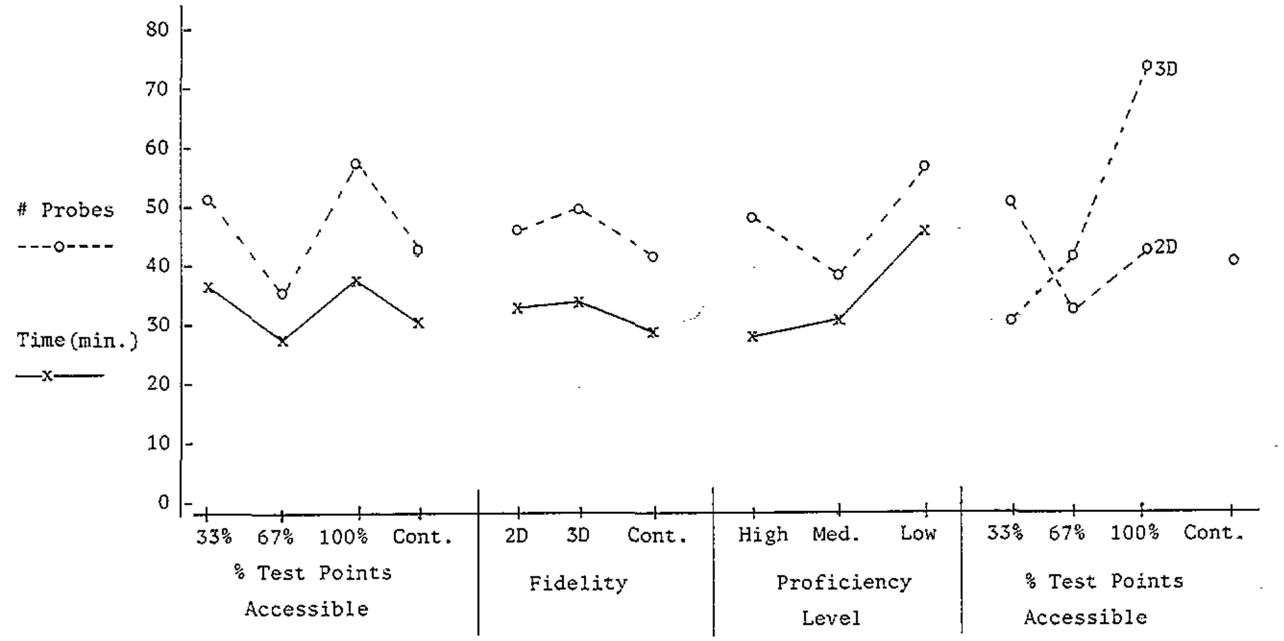

Figure 4 Probes and Time By Experimental Condition

and 3D boards. This difference was not statistically significant. High proficiency students located the fault in significantly less time (p=0.056), but number of probes was not significantly affected by proficiency.

There was a significant interaction (p=0.01) between fidelity of simulation and percent points accessible during training on number of probes in testing. Students trained on two-dimensional boards with 67% of the points accessible had the fewest number of probes in testing.

Troubleshooting Success

A Chi Square Analysis of student troubleshooting success (see Table 2) found no significant difference (p=0.17) in fault diagnosis success rate between students trained on two-dimensional, three-dimensional and unmodified boards. There was also no significant difference (p=0.59) between students trained on unmodified boards and those trained with 33%, 67% and 100% test point accessibility.

Table 2

Fault Location Success Rate
By Board Type In Training

	Correct First Time Yes	Correct First Time No		Correct First Time Yes	Correct First Time No
2D	19	10	33%	12	5
3D	11	16	67%	10	11
Control	4	3	100%	8	10
			Control	4	3

Troubleshooting Logic

The specific points probed by students during performance tests were analyzed in order to provide guidance to engineers in selecting which points students are most likely to probe. Analyses addressed troubleshooting logic and characteristics of points probed.

The sequences of probes for each of the performance tests were analyzed to determine which troubleshooting strategies were utilized by the students. Results appear in Table 3. Definitions of these strategies are:

Half-Split	Testing the midpoint between good and bad signal until fault located
Linear I/O	Testing output of each circuit
Linear Tracing	Testing components sequentially until faulty signal found
Reliability Testing	Testing least reliable untested component
Symptomatic	Testing based on equipment symptoms
Random	No logical sequence of tests
Combination	Use of two or more strategies

Since the dominant strategy is random probes, no rules can be recommended for selecting active test points based on troubleshooting strategy.

Table 3

Troubleshooting Strategies Utilized

Strategy	Times Utilized
Half-Split	1
Linear I/O	6
Linear Tracing	2
Reliability Testing	5
Symptomatic	3
Random	25
Combination	18

An analysis of characteristics of the printed circuit board components tested by students was conducted in order to determine whether the characteristics of components affect the frequency with which they are probed. Table 4 contains the results of this analysis.

Table 4

Test Point Probes
By Component Characteristics
Expected Versus Observed Frequency

Characteristic	Type	Expected Probes	Observed Probes	Difference (%)
Electronic Location	Input	201	125	-38
	Middle	100	210	+101
	Output	297	346	+16
	Other	3583	3509	-2
Electronic Circuit Location	Input	498	458	-8
	Middle	100	201	+101

Table 4
(Cont'd)
Test Point Probes
By Component Characteristics
Expected Versus Observed Frequency

Charac-teristic	Type	Expected Probes	Observed Probes	Differ-ence (%)
	Output	498	462	-7
	Other	3085	3060	-.8
Physical Location	Edge	1793	2025	+13
	Middle	297	514	+73
	Other	2091	1642	-21
Size	Large	698	970	+38
	Small	3483	3211	-7

If students test components without regard to their characteristics, then the expected proportion of probes associated with each component will be equal to the proportion of test points associated with that type of component. A Chi Square Analysis of expected versus observed probe frequency found the differences to be significant ($p > 0.01$) for all component characteristics.

Students test the midpoint in the board circuitry as the first step in a half-split technique, but they do not continue this procedure until the faulty component is located. The board output is tested more often than the input. The physical midpoint was near the electronic midpoint and shows the same trends.

Once a circuit on the board is suspected of being faulty, the student predominantly probes the midpoint of the circuit, as opposed to the input or output. Finally, students are more likely to test a large component than a small one.

CONCLUSIONS

Basic electronics training on circuit boards with reduced physical fidelity and reduced test point accessibility is equal to or superior to training on unmodified actual circuit boards. Students trained on two-dimensional boards with 2.75 times as many test points available as required had the best overall troubleshooting performance during testing.

Other than the minimum points specifically required to detect a fault, the following points should be accessible on a simulated board:

- Electronic Midpoint of Board
- Board Outputs
- Electronic Midpoint of Circuit
- Test Points Associated With Large Components

ABOUT THE AUTHORS

Dr. Bruce McDonald is a Senior Human Factors Engineer and President of McDonald & Associates, Inc. He specializes in the areas of maintenance training and training equipment front-end analyses. He holds a Ph.D. degree in Industrial Engineering from Texas A&M University and an M.S. degree in Experimental Psychology from North Texas State University.

Ms. Grace P. Waldrop is an Associate Human Factors Analyst and a Project Director at McDonald & Associates, Inc. She is involved in research projects on maintenance training, helicopter night vision systems and Naval war gaming. She holds an M.S. degree in Industrial Psychology from the University of Central Florida.

Dr. Richard E. Reynolds is an Experimental Psychologist with the Human Factors Laboratory, Naval Training Equipment Center. He is involved in Maintenance training, surface warfare training and aircrew training. He holds a Ph.D. degree in Experimental Psychology from Miami University.

The authors wish to acknowledge the valuable assistance of Virginia T. White in gathering and analyzing data, Rickard L. Romanenko in providing electronics assistance, and Connie Thomas for assistance in data analysis and manuscript preparation.