VHSIC FOR TRAINING SYSTEMS

David P. Glenn
Naval Training Equipment Center
Orlando, Florida

Harold T. Freedman
Honeywell Inc.
West Covina, California

Dr. James A. Gardner
Honeywell, Inc.
West Covina, California

ABSTRACT

Very High Speed Integrated Circuits (VHSIC) is a new technology which promises to have a major impact on the training and training device community. As DoD and industry, in a joint effort, began to pursue this technology in 1980, it quickly became obvious that VHSIC, if successful, would result in more than just an evolutionary change in microelectronics -- it had the potential to revolutionize the way in which we design, build, and use electronic devices. At this point in 1983 the performance predictions for the VHSIC technology are very close to being achieved. Not only will we have available to us significant increases in processing throughput, but the VHSIC chips will be smaller, lighter, require less power, and be more reliable than their predecessors. Cost savings are also predicted. As these advantages came close to reality in 1982, the Naval Training Equipment Center recognized a tremendous potential in the new chips to improve the future training devices and solve some problems being presented by the limitations of current technology. Therefore, a study contract was let to Honeywell (one of the six DoD VHSIC contractors) to investigate the impact of VHSIC on training and training devices. This paper will discuss the results of that study and indicate the future direction in which the VHSIC technology will drive the training community.

INTRODUCTION

The DoD VHSIC program was established to provide focus and resources to overcome the limitations of silicon IC technology, and has far reaching implications relative to the security of this nation. Not only is VHSIC the next logical step to maintain technological leadership in microelectronics, but its application to military hardware will provide a distinct advantage in fielding more sophisticated military systems. However, as one begins to understand the tremendous improvements allowed by the VHSIC, it becomes obvious that our new weapons systems are not the only potential benefactors of the new technology. Indeed, the VHSIC advantages can be applied to almost any electronic device and have the potential to make significant impacts throughout both military and civilian arenas. Its not just a matter of accomplishing the same electronic function in a more efficient manner. The VHSIC will allow us to push back the existing electronic design boundaries and accomplish new roles which were heretofore beyond the limits of our technology. We can, therefore, expect to see impacts on how we operate, maintain, and use the new electronic devices made possible by the VHSIC development.

Since the Naval Training Equipment Center is charged with responsibility to develop, procure, and support Navy training systems, the DoD plan to push the VHSIC technology is viewed with both excitement and apprehension. After all, it is easy to envision the VHSIC as not only a better way of building the traditional training device, but also a technology that will facilitate and even demand new approaches to training. With these thoughts in mind, it became necessary to do some research and analysis into the VHSIC impact on training in order that a future course of action may be charted to allow preparation for a full exploitation of the new VHSIC technology. That was the purpose of the Honeywell study, the results of which are reported herein.

In order to make this paper understandable to those who may not have carefully followed the VHSIC development, we have included a synopsis of the DoD VHSIC program. The goals and approach of the study will then be described, followed by the results. There has been an attempt to chart a direction for VHSIC insertion into training devices which involves the development of a Training Chip Set (TCS). Plans for the TCS include the objective to make the chips available to all training systems designers without providing any competitor a major advantage in the marketplace.

VHSIC - WHAT IS IT?

Overview of VHSIC Program

The DoD's VHSIC program was divided into several phases over a six-year period, beginning in March 1980.

During Phase 0 of the program, March to November 1980, nine contractors were selected to develop concepts and brassboard chip projects that would best meet the long-term objectives of developing new microelectronic technology and devices that are geared to the specific constraints of defense systems. As a result of the Phase 0 study, six contractors have been awarded Phase 1 contracts to take their concepts to reality by mid-1984. A Phase 2 program was awarded in August 1981 with the objectives of (1) yield enhancement, (2) technology insertion, (3) sub-micron technology development, and (4) developing integrated design automation systems. In concert with the Phase 1 and Phase 2 efforts, Phase 3 of the program (1980-1986) provides the supporting research effort in the form of a large number of small contracts (60 contractors) to enlist the innovative research and development efforts of the much broader community of researchers in industry, universities and research institutions. A summary of the VHSIC program schedule is shown in Figure 1.

The objective of the VHSIC Phase 1 program is three-fold. The first is to design, fabricate, and test 1.25 micron geometry integrated circuits (IC's), with a minimum functional throughput rate (FTR) of 5 x 10" gate - Hertz per square centimeter. The FTR is a product of gate density and speed. The second objective is to demonstrate a pilot line capability to produce VHSIC chips. The third objective is to deliver brassboard chips to demonstrate VHSIC performance. insert VHSIC into other military applications.

The VHSIC Phase 2 program procurement is currently underway. The original plan was to extend the limits of the 1.25 micron technology to sub-micron feature sizes. However, the experience gained from the VHSIC Phase 1 program thus far has shown that the 1.25 micron technology will yield sufficient benefits to numerous military system applications to support continued development.

The current emphasis for Phase 2 seems to have three major objectives. The first one is to facilitate VHSIC technology transfer. This involves efforts to encourage VHSIC Insertion into various weapon systems. Second, achieve IC pilot line certification and to reduce chip costs. The third objective is to develop the sub-micron process technology.

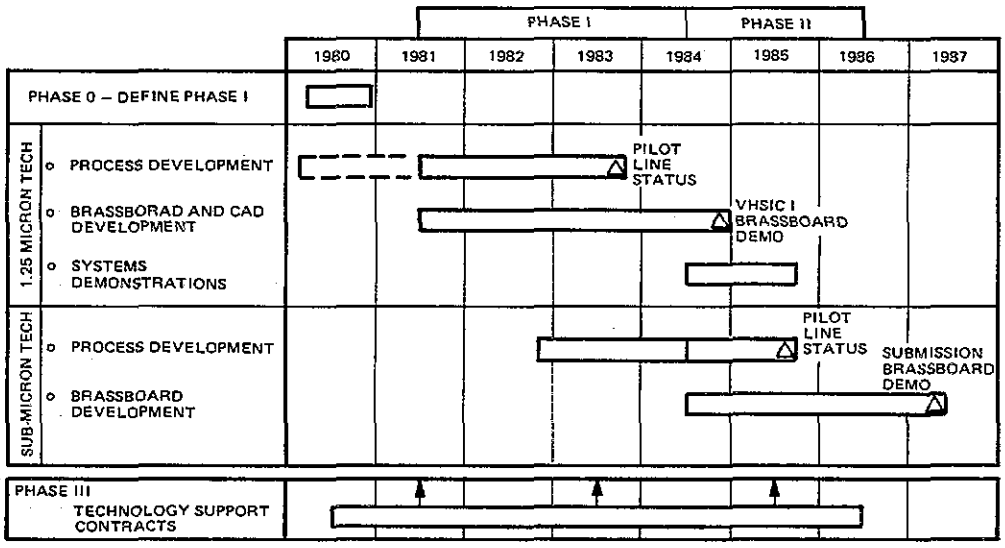

Figure 1. VHSIC Program Schedule

Currently, the overall status of the VHSIC Phase 1 program can be summarized as follows:

- o Design verification is in progress
- o Chip design is in final revision
- o Device and process characterization is in progress
- o Brassboard design is underway

A summary of the characteristics of the chip sets and brassboards that are currently being developed for VHSIC Phase 1 is shown in Table 1.

VHSIC Technology Issues

As the VHSIC Phase 1 program proceeds along with the chip development efforts, both the VHSIC contractors as well as the potential users are beginning to investigate and address the various issues that must be resolved to make VHSIC technology widely applicable to the DoD community. These issues can be grouped into three main areas:

- o Interoperability
- o Support Environments
- o Procurement Options

Each of these issues has a significant impact on the user of VHSIC technology. Without chip interoperability among the six contractors, the design of any system may be constrained to the use of chips from one manufacturer. In addition, VHSIC chips will be more easily accepted if a user-friendly software support environment is available. Finally, unless the technology can be made readily available in a variety of manners (i.e., transferable), potential users, other than the original may be faced with problems that could make the use of VHSIC unattractive.

Table 1. Summary of VHSIC Phase 1 Contractor Approaches (Excerpt from IEEE Spectrum, December 1982)

Contractor (Service)	Technology	Brassboard	Design Approach	Chip Set	Special Features
Honeywell (Air Force)	Bipolar ILS*, CML#	Electro-optical signal processor	Custom chip based macrocell library	Parallel programmable pipeline Controller	Radiation hardness Responsive generic architecture
Hughes (Army)	CMOS on SOS	Anti jam communications	Standard and custom reconfigurable chips	Digital correlator Algebraic encoder/decoder Spread-spectrum subsystem	Radiation hardness Electron beam direct-write lithography Highly specalized chips
IBM (Navy)	NMOS	Acoustic signal processor	Master image with macrocell library	Complex multiplier/accumulator	Software strength Design approach
Texas Instruments	Bipolar STL## NMOS	Multi-mode fire-and-forget missile	Programmble chip set	Data processor Array controller and sequencer Vector address generator Static RAM Multi-path switch Device interface unit General buffer unit	Operational fabrication facility Design utility system
TRW (Navy)	Bipolar-3D** TTL, CMOS	Electronic-warfare signal processor	Standard chip set	Content addressable memory Window addressable memory Registered arithmetic logic unit Address generator Matrix switch 15-bit muliplier/accumulator Micro-controller Four-port memory	Innovative memory chips Versatile chip set
Westinghouse (Air Force)	Bulk CMOS	Advanced tactical radar processor	Standard chip set unit	Pipeline arithmetic unit Extended arithmetic unit Controller Gate array Static RAM Mutiplier	Highest speeds

* Integrated Schottky logic, #Current mode logic, ##Schottky transistor logic, **Triple Diffusion

VHSIC Interoperability Issues. The six VHSIC Phase 1 contractors are all working very hard to develop and fabricate their respective chip sets and brassboards. Each is developing one of the competitive IC technologies -- NMOS, bulk CMOS, CMOS on SOS, and bipolar -- to the design and fabrication of chips. Due to the nature of the VHSIC program, each contractor is working independently. Outside of initial program objectives, little consideration has been given to the issue of interoperability; i.e., how VHSIC chips of different manufactures can be used in the same system. The need for some form of standardization among the VHSIC chips is beginning to be recognized and different committees and action groups have been set up to look into these issues and to recommend possible solutions. In particular, three topics are currently being pursued: bussing, power supply voltages, and packaging. Committees have been set up to provide guidance and standardization to the individual developers.

To resolve these questions, a VHSIC interconnect standards committee (V-BUS) has been formed, with participants from all six VHSIC contractors and the user community.

VHSIC Support Equipment. The VHSIC Support Environment needs can be divided into two major areas: support of software tools and support of Computer Aided Design tools.

Software Support. The software support tools development effort is directed at two levels:

- o High Level - Ada programming support
- o Low Level - Microcode compiler

DoD has identified Ada as the standard high order language for use in the future. All the VHSIC chips have been designed to be compatible with this requirement. Two programs are currently in progress to define and develop the Minimal Ada Programming Support Environment (MAPSE). The first one, called Ada Language System (ALS), is let out of the Army (CECOM) to Softech. The effort is hosted on a VAX-700/VMS and is scheduled to be completed by January 1984. The second effort, called Ada Integrated Environment (AIE), is let out of Air Force (RADC) to Intermetric. The system is hosted on IBM 370/VM and is due at the end of 1984.

Table 2 shows the tools for use in Ada Programming as a result of the two programs.

While these two efforts are going on, there are already available in the commercial market less sophisticated compilers for subsets of Ada. These tools can be very useful for learning Ada and for training Ada programmers.

Table 2. Ada Support Tools

KAPSE	(Kernel Ada Programming Support Environment)
	Virtual Support Environment
	I/O Support
	Data Base Support
	Operating System Support
MAPSE	(Minimal Ada Programming Support Environment)
	Text Editor
	Prettyprinter
	Translator
	Linkers
	Loaders
	Analysis Tool
	Terminal Interface
	File Administrator
	Command Interpreter
	Configuration Manager

For VHSIC chips to be microprogrammable, microcodes have to be prepared. In order to generate microcodes efficiently, a microcode compiler is needed. Currently each VHSIC contractor has his own approach to preparing the microcodes for his particular VHSIC chip architecture design.

At Honeywell, a microcode compiler for the EOSP chip set has been completed. It uses a high level Ada-like language called HML. The compiler is hosted on a VAX/780. In the near future, there are plans to extend the capability of the microcode compiler to enable it to be retargetable to other architectures more conveniently, to extend the versatility of the language (HML) and to generate more optional code.

A versatile and efficient microcode compiler is essential as VHSIC chips find wider applications.

Computer Aided Design Support Tools. One of the side benefits of DoD's VHSIC programs is the development of various CAD support tools. In order to successfully fabricate VHSIC chips, the VHSIC contractors had to upgrade their CAD systems to meet VHSIC Phase 1 goals. These CAD tools will then be delivered to DoD to support the future development of ICA's.

At Honeywell, the CAD system utilities for VHSIC is called the Advanced Integrated Design Automation (AIDA) system. The development of the AIDA system can be divided into two stages. The first stage (AIDA I) has been completed and is being used for the VHSIC Phase 1 design. In the AIDA I system, the data base is in the form of a collection of files. The second stage (AIDA II) is expected to be completed by the end of VHSIC Phase 1 and is to be a VHSIC Phase 1 deliverable to the Government. For AIDA

II, there will be an integrated data base which will facilitate the design process via remote design centers.

The Honeywell AIDA system is based on a hierarchical approach with the design process dividing into various levels, namely; gate, macrocell, functional blocks, chip and system levels. With the incorporation of an integrated data base system and one single hardware description language (HDL), the AIDA system will be a very powerful and versatile CAD support tool system for VHSIC.

Procurement Options. One of the questions that is frequently brought up is that of procurement options; that is, how is the VHSIC technology to be made available to the various users? To answer this question, each VHSIC contractor has to formulate an approach to answer this question.

A typical approach to accomplish this objective is to provide a full range of services ranging from sale of chips to various design and processing options. This may be further facilitated by some developers design approach which includes the use of a macrocell type design methodology, a complete CAD system, and distributed design centers.

The VHSIC design and processing functions can be illustrated by the flow diagram shown in Figure 2. The VHSIC chip development process can be divided into five stages: conceptual design, system design, chip design, processing, and finally packaging/testing.

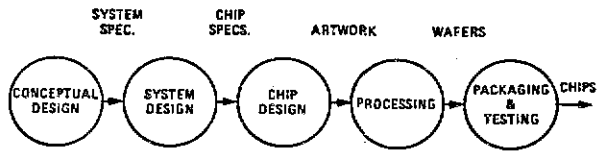

Figure 2. VHSIC Design and Processing Functions

It is conceivable that with this approach the developers could provide four different service options to the VHSIC users. They are described as follows:

Option 1. The conceptual design could be performed by the customer. The VHSIC supplier will provide the customer with the necessary VHSIC technology: performance descriptions, power requirements, and VHSIC library listings. The customer will then generate the appropriate systems specifications and the VHSIC supplier will perform the rest of the design and processing functions.

Option 2. The customer will perform both the conceptual design and the system design. In addition to the VHSIC technology description, the VHSIC supplier may also provide the customer with access to their VHSIC chip library, the macrocell library if available, and the necessary CAD tools for system design. The customer will then generate and provide to the supplier the chip specification for chip design, layout mask fabrication, processing, packaging, and testing.

Option 3. For this option, all the design work could be performed by the customer, with the VHSIC supplier providing the necessary design rules, access to the macrocell library, and CAD tools for chip design. The customer will then generate and present the supplier with the appropriate digitized layout tape and test and design check tools. The supplier will do the IC processing, packaging, and testing.

Option 4. For this option, the VHSIC supplier would provide a silicon foundry service whereby they will receive from the customer the necessary artwork tape to fabricate and process the VHSIC IC's. The customer will perform all the design work, and will get back from the supplier the processed wafers. The customer will provide for their own packaging and testing functions.

VHSIC Status Summary

Those elements of the status above which are relevant to the insertion of VHSIC technology into operational equipment and training devices are:

- The Phase 1 developed 1.25 micron geometry IC's are directly applicable to military systems -- including training devices.
- One of the Phase 2 submicron objectives is to provide VHSIC Insertion into Weapon Systems.
- An interoperability concern exists with the IC's being developed by the six different contractors which is presently being jointly addressed by the Phase 1 contractors with the VHSIC Phase 1 office.
- Software support is also unique for each of the six contractors.
- IC's can be procured in a variety of manners -- from preparation of system design concept specifications through the ordering of 'standard' chips.

The status of the VHSIC program can be summarized as follows: VHSIC as a technology is here, the problems have been clearly defined, and solutions are being developed. VHSIC as a culture has not yet

been examined by the majority of the users. The question before us is what are the impacts, and how do we respond?

The implication of VHSIC to trainers is shown in Figure 3. VHSIC as inserted into weapon systems will impact both the system capabilities and employment, thus requiring new training requirements and approaches. VHSIC as inserted into Maintenance, will allow new trainer concepts and capabilities. Both avenues of VHSIC Insertion impact will result in improved training.

THE VHSIC FOR TRAINING SYSTEMS STUDY

The objectives of the study performed by Honeywell's Training and Control Systems Operations were to identify the impact VHSIC would have on Training Systems, and to develop an approach for coping with this new technology. The impetus to the study was to answer the questions "VHSIC is here, how do we respond?" It was felt that we need to prepare for the training impact caused by VHSIC insertion into Weapon Systems, platforms, we need VHSIC to solve some persistent high priority training problems and training must take full advantage of the new technology.

Specifically, the goals of the study were:

- Identify classes of operational equipment for which VHSIC technology is considered appropriate, that is, VHSIC Insertion candidates.
- Select specific candidates to explore in general terms the impact of VHSIC Insertion on operation and maintenance.
- Evaluate the skill changes for these candidates for use in determining the impact.
- Identify the changes in training requirements which will be necessitated by VHSIC insertion into operational equipment.
- Identify those training requirements which result from persistent training needs.
- Identify the training device requirements which will be needed to support the evolving training requirements.

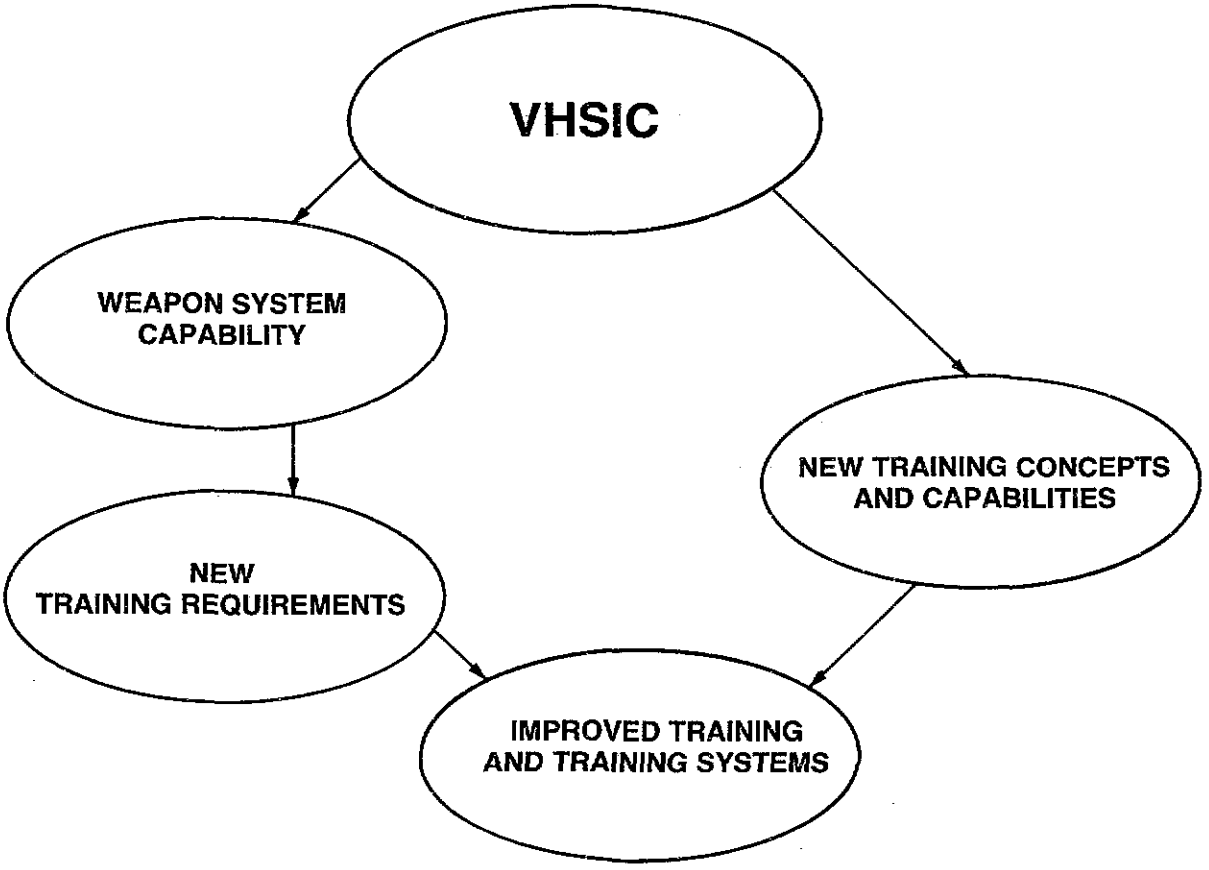

Figure 3. VHSIC Relationship to Training

- Develop an application approach to meeting the new training needs.
- Characterize a concept which results from the approach.
- Identify recommendations related to further development of the concept.

VHSIC Technology Impact on Operational Equipment

The determination of the impact of VHSIC technology insertion into operational equipment was made to identify the skills necessary to operate and maintain VHSIC based equipment. Figure 4 illustrates the major milestones in the VHSIC program. The approach to skill identification was conducted in two phases.

The first phase identified the classes of operational equipment for which VHSIC technology is considered appropriate, that is, VHSIC Insertion candidates. The second phase identified the types of skills or changes in skills necessary to operate and maintain the insertion candidates.

The results of the second phase indicated that skill changes will occur for three types of personnel: equipment operators, maintenance technicians, and operator teams.

Equipment Operator Skills:

- Proficiency on several pieces of equipment
- Increased tactical decision capability
- Decreased equipment manual operation
- Addition of simple maintenance skills

Maintenance Technician Skills:

- Two skill levels will be required:
  - Operator/Maintainer to interpret BIT displays and perform remove and replace tasks
  - Expert technician to perform tasks beyond the level of BIT repairs

Operator Team Skills:

- Increase in shared tactical responsibilities
- Increased emphasis on communication and coordination
- Emphasis on skill retention

VHSIC Technology Impact on Training

The development of VHSIC technology has prompted the Naval Training Equipment Center to identify two important issues driving changes in training requirements:

1. The need to prepare for the training impact caused by the use of VHSIC technology in weapon systems platforms, and
2. The solution of some of the persistent problems which have inhibited effective training.

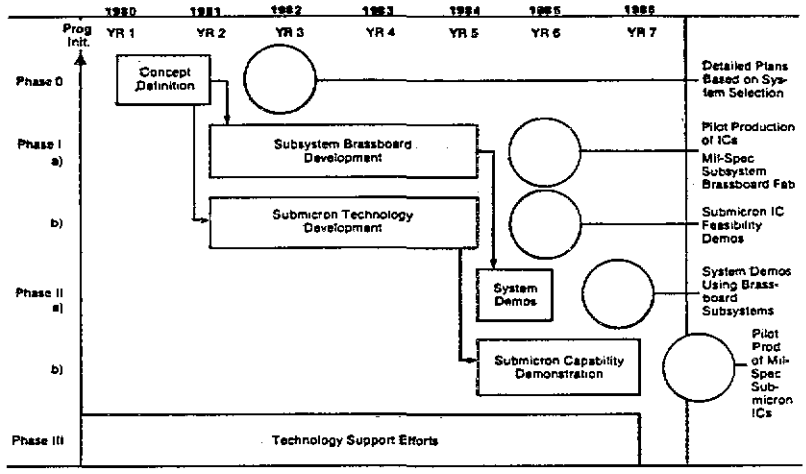

Figure 4. Milestones for DoD VHSIC Program (Take from Military Electronics/Countermeasures, December 1981)

The approach to identifying changes in training requirements was as follows:

- Identify the changes in training requirements necessitated by VHSIC insertion into operational equipment.
- Identify training requirements resulting from persistent training problems.
- Specify the training device requirements needed to support evolving training requirements.

The training changes identified (Figure 5) to accommodate skill changes for equipment operators, maintenance technicians, and operator teams were as follows:

Equipment Operator Training:

- From less emphasis on routine tasks to more emphasis on quick decision making.
- More emphasis on cross-training to acquire multiple equipment skills.

Maintenance Technician Training:

- More emphasis on simple mechanical skills to support equipment maintenance at a BIT interpretation and remove-and-replace repair level.
- Basic technician will be replaced by an Operator/Maintainer.
- The expert technician will receive more emphasis on complex trouble-shooting, detailed fault isolation, and in-depth system understanding and theory of operation.

Operator Team Training:

- More emphasis on communication and coordination skills to support team training.
- More wargaming exercises.

VHSIC will, therefore, significantly change the roles of equipment operators and maintainers. With the significant increases in weapon system computing power and speed, coupled with the significant reductions in electronic assembly size, operators will now become more tactical decision makers, and maintainers will follow more structured and automated checkout procedures. The following is a summary of such predicted changes.

Offensive Weapon System Role Changes. As a result, future offensive weapons will be autonomous after launch (i.e., fire and target), and, in the distant future, even before launch. Weapon autonomy will improve the survivability of the launching platform due to the shortened exposure time.

In addition, VHSIC based weapon systems will be more reliable, easier to maintain, and have a higher inherent availability (Ai). These improvements will be due to the high reliability of VHSIC chips, the decreased size and number of components which result from VHSIC insertion, and a more extensive use of Built-In-Test Equipment (BITE).

The use of more BITE will improve the maintainer's ability to isolate and replace faulty components or units. Size and quantity reductions will reduce the

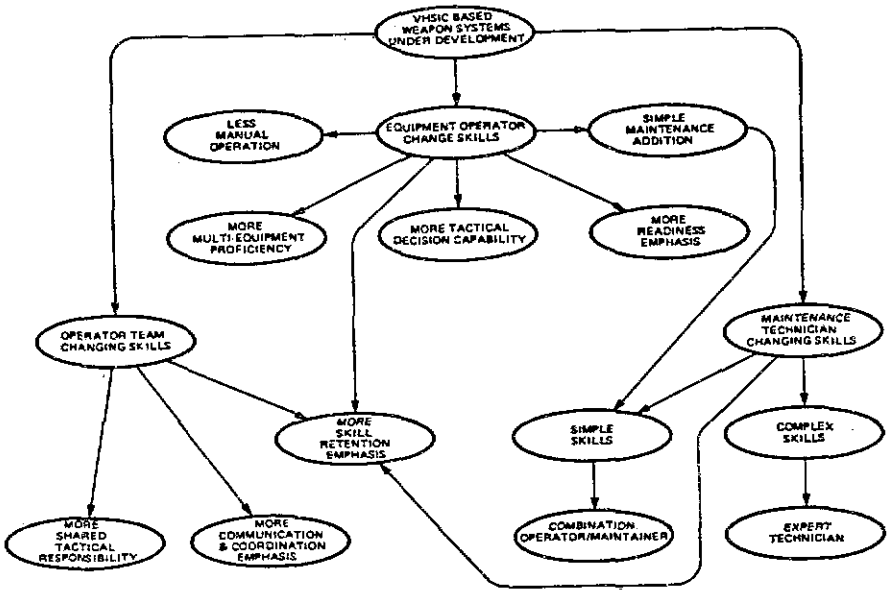

Figure 5. Roadmap for Skill Changes

time to repair, higher reliability will decrease the failure rate, and thus Ai will increase.

Role Change for the Offensive Weapon Operator. The change foreseen in the offensive weapon operator role will be from that associated with weapon control to that associated with a tactical decision capability. The time gained through the use of a fire-and-forget type munition will be used for combat scenario assessment, multiple target selection, survivability tactics, etc.

Role Change for the Offensive Weapon Maintainer. The change foreseen in the role of the offensive weapon maintainer will be from that associated with troubleshooting and repair to that associated with interpreting BIT indications and performing routine remove and replace actions. Cases beyond BIT fault isolation, although relatively fewer in incidence, will require more knowledge and skill on the part of the maintainers.

Role Change for the Offensive Weapon Team. This change will require a higher degree of shared tactical responsibility -- a trend now evident in modern weapon systems.

Defensive Weapon System Role Change. Major conflicts in the future will be manifested by multiple threats from different enemy platforms. The positive, early detection of such a scenario can be enhanced through the use of defensive systems which are capable of detecting, acquiring, classifying and tracking a large number of threats. The use of VHSIC technology can provide the data processing power necessary to automate all of these functions.

Role Change for the Defensive System Operator. The role change foreseen for the operator of a defensive system, such as a search and surveillance radar, will be from a control manipulator to a tactics decision maker.

In addition, it should be possible for one operator to oversee several pieces of automated equipment. This capability will reduce manning requirements and/or serve as a casualty response during battle.

Role Change for the Defensive Weapon Team. The defensive weapon team role will change from a detection/reaction role to a more effective reaction role which is responsive to multiple threat scenarios. This change will require better communication and coordination between members of a weapon system and between teams aboard a multi-weapon system platform.

Impact on Training and Training Devices

As VHSIC is introduced into the weapon system design, the above changes in roles are forecast to result. These will, in turn, necessitate changes in the training techniques and devices used to support the weapon systems. It is not a direct conclusion that training and training devices will become more complex. Rather, they will employ different features and functions which are not necessarily more difficult to simulate. Since simulators generally simulate only what is seen by the operator, not how the equipment functions, training devices may, in fact, become simpler. Because the weapon system will process many more sensor inputs, reduce the data to a summay form and require decision making on the part of the operator, the simulated information presented to the trainee may be less complex than today's training devices.

In the case of stimulated training devices such as sonar systems having synthetically generated signal sources driving an operational equipment mockup, the training device design may also be simpler. Through the use of VHSIC components in the design of the training device, ocean and target modeling may, in fact, be simpler than today. Computational bounds on speed and size may be resolved through the use of VHSIC components in new distributed architectures.

It is, therefore, anticipated that the introduction of VHSIC into weapon systems will not make the training system design more difficult. It will, however, be different and we must anticipate these impacts in our training system requirements and designs. We must stay abreast of the technology advances to ensure that training systems ensure student and weapon system readiness.

The concluding part of the study was conducted to identify how VHSIC technology can be applied to the design of training devices. The approach to application was:

- Identification of appropriate VHSIC attributes.
- Selection of VHSIC Insertion training device candidates from the identified training device needs.
- Development of an application approach.
- Characterization of a concept which resulted from the approach.
- Identification of recommendations related to further development of the concept.

This approach led to specific VHSIC application areas, to a generic method of providing VHSIC Insertion cost effectiveness to the selection of a prime candidate training system, and to a set of recommendations for the pursuit of achieving VHSIC insertion into training devices.

The conclusions of the study identified specific areas where VHSIC could benefit the design and performance of training devices. These benefits were primarily in the areas of size, speed, cost, and reliability.

The reduced size of VHSIC IC's currently in development (1.25 micron feature size) permits a veriety of new applications and capabilities. Today's complex system trainers such as flight simulators, tactics trainers, and ASW trainers involve many racks of electronic equipment. This large hardware complement requires significant dedicated facilities, cooling, and power. Through the introduction of VHSIC components into the system design, significant reductions in equipment size, even approaching or exceeding fifty percent, are possible by the late 1980's. These hardware reductions will also impact system and facility support costs through reduced maintenance, cooling, and power requirements.

The use of VHSIC components will impact system cost by combining many different circuit functions on a single chip. This, in turn, will reduce the number of circuit boards, card frames, and equipment racks. Distributed processing designs will be both practical and cost effective. However, it remains questionable whether true system cost savings will be achieved due to the increased functionality possible. It is likely that the added computing capability possible with VHSIC will be used to enhance the training device effectiveness, thus making up for the inherent cost reduction through more compact, efficient system design.

There exists today a variety of persistent high priority training problems which cannot be solved with today's VLSI technology. The sheer amount of computations for many of today's training devices limit their ability to realistically perform in real time. NTEC has identified eight training device areas which are presently capacity or speed limited by current technology:

1. Dynamic Target Modeling
2. Real Time Scenario Event Control
3. Intelligent Adversary Modeling (Responsive Targets)
4. Computer Aided Instruction (CAI) and Computer Managed Instruction (CMI) Modeling
5. Environmental Modeling
6. Acoustic Modeling
7. Image Scene Generators
8. Organic (Built-in) Training Capabilities in Tactical Equipment

Through VHSIC, it will be possible to significantly increase the realism of weapon system trainers through more detailed real time computation and simulation of the operational environment. The limitations of size and speed have precluded effective organic training. These same problems have limited the development of highly effective, field-portable training devices. Tactical environments and power constraints have limited the use of large portable vans in the field. Through VHSIC, small hand-held portable devices can be displayed which will provide highly effective training. Both organic and strap-on training approaches will become a practical reality. As the use of Artificial Intelligence (AI) technology emerges into an application phase, VHSIC technology will become an integral part of the AI application into training devices. VHSIC will significantly aid the training system designer in meeting the evolving needs of future weapon systems.

Through the study, it emerged that a high payoff area for the introduction of VHSIC into training systems was in the area of visual simulation systems. In computer image generation (CIG), a present limiting factor to the number of polygons (image detail) generated is the ability to process in real time the various algorithms making up the simulated image. Through the use of VHSIC hardware and architectures, it will be possible to significantly improve image resolution and quality. It was recommended that this area be explored further as the first candidate application of VHSIC.

It was determined in this study that a generic core set of VHSIC chips could meet the requirements of a large majority of training devices. Through an examination of common computation/processing requirements found in a variety of different training device applications, a common core of VHSIC chip requirements was identified. This common core, called the Training Chip Set or TCS, was further defined to determine its optimal configuration to meet this diverse range of training device applications. A key conclusion of the study was, therefore, the need for the development and application of this generic chip set to training devices.

THE TCS - WHAT IS IT?

The approach to the TCS concept was based upon measurable design and development goals.

Design Goals

Three design goals were established.

Performance. The measure of performance was taken as data throughput expressed as Millions of computer Instructions Per Second (MIPS). The goal was to achieve an order of magnitude greater than that for devices using conventional technology, with an absolute goal of not less than 10 MIPS.

Size. The goal was to reduce by an order of magnitude the volumes of conventional devices. This change in size would permit desk-top simulators which now occupy cabinets, or from a desk-top size to a hand-held device.

Cost. The goal was to achieve a 50 percent reduction in the Life Cycle Cost (LCC) of conventional technology based devices.

Development Goals

The following four development goals were considered.

1. A single development effort should be pursued to achieve a universal set of VHSIC chips applicable to training devices. The benefits are obvious: lower cost and higher priority position in a critical technology.

2. The chip design should have the capability to provide functionality for all foreseen applications. In addition to meeting the needs of the entire instructional environment, the designs should not be platform unique (i.e., only classroom trainers).

3. The chips and the design process should be available to the entire training community. This includes Joint Service access and use by all device designers.

4. The design of the chips should fully incorporate existing VHSIC technology. This includes not only specific chip designs, but also design techniques and tools, fabrication techniques, and testing techniques.

The identification of this set of goals set the stage for the major effort of the study -- the VHSIC implementation technique.

VHSIC Implementation

The benefits of VHSIC technology to training devices are profound and numerous. However, successful insertion of VHSIC technology into training systems will have to be made in a timely and cost effective manner. The Training Chip Set (TCS) concept developed under this study allows the insertion of VHSIC technology into a variety of Training Systems at a reasonable initial cost and minimal marginal cost.

The goals of developing a TCS were:

1. Modularity to allow application to various current systems and to allow expansion to future training systems.

2. Separation of functions to simultaneously allow flexibility (i.e., programmability) and high throughput.

The training chip set concept is depicted in Figure 6. For any given training system, the TCS will consist of two major portions: the core controller and the adjuncts specific to that particular training system.

The insertion of VHSIC technology into a particular training system will consist of several core controllers (each of which consists of several VHSIC chips as described later) and a much larger number of adjuncts (each one of which will be typically implemented using a single VHSIC chip). In this configuration, each core controller will control several adjunct chips. The number of adjuncts which can be controlled by a core controller depends upon data rates in a specific training system and will typically vary for different training systems.

The core controller is highly programmable and thus allows flexibility to accommodate changes and updates in the functioning of the training system. The adjunct(s) are directly in the path of the data flow and provide very high throughput operations on the data. Thus, the goal of high throughput together with programmability is achieved.

Under this study, we have evaluated the applicability of the TCS concept to two training systems. These are:

1. Computer Generated Synthesized Imagery (CGSI).

2. Anti-Submarine Warfare Trainer (ASW Trainer).

The CGSI system is being developed for more realistic visual training and the use of VHSIC technology will allow real-time operation of a complex, multi-channel CGSI system. The ASW trainer is the traditional sonar trainer and the insertion of VHSIC technology will dramatically reduce the size of sonar trainers.

Preliminary design of a one chip CGSI adjunct VHSIC chip and a one-chip ASW adjunct have been completed. Preliminary estimates show that a controller, implemented using four VHSIC chips, will be able to control up to 100 CGSI or ASW adjunct chips.

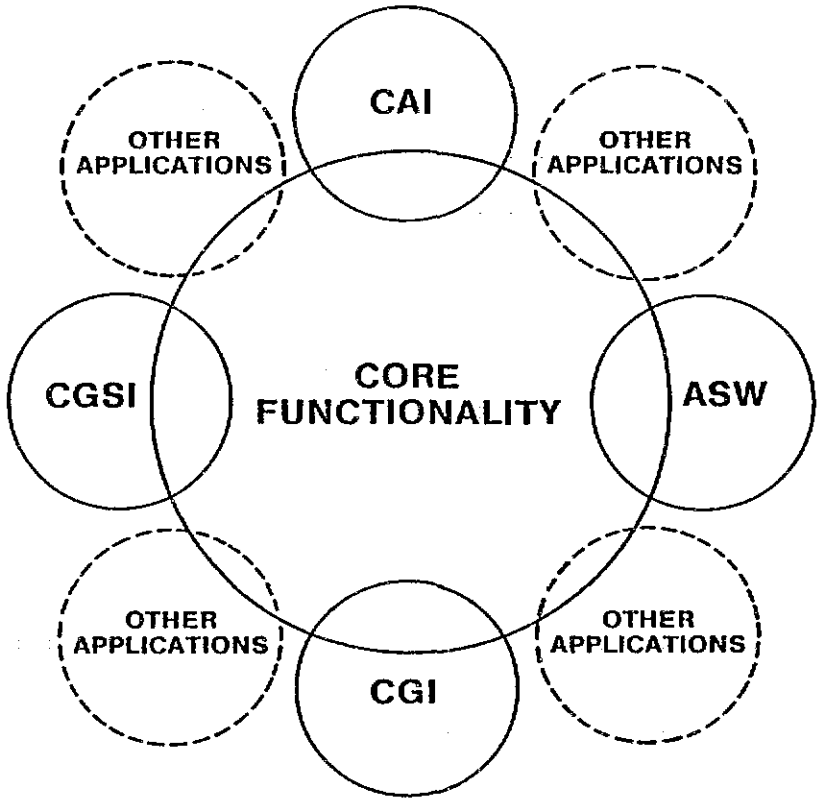

Figure 6. Training Chip Set Adjunct Concept

The modular approach to the TCS will allow the application of VHSIC technology to other training systems by using the controller and new adjunct(s) specifically designed for these training systems. Thus, the meaningful cost of inserting the VHSIC technology into future training systems will be drastically reduced.

SUMMARY

The primary goal of the NTEC VFTS study was to determine the impact of the DoD VHSIC program on weapons systems, training and training devices and to derive a comprehensive impact assessment. This goal has been achieved and, in addition, the concept of a VHSIC Training Chip Set (TCS) evolved as the study progressed.

The availability of proven VHSIC components for insertion in weapon systems can occur as early as 1986. New and different training devices and training capabilities will be required to meet the training needs of the future; the Training Chip Set -- can meet the requirements of a large majority of these requirements.

Increased system performance of VHSIC technology provides the forecast of increased system performance and reliability in diverse application. Both training requirements and trainers will change. In particular, performance, physical characteristics and projected cost of VHSIC technology under development will significantly improve present and future training devices. This basic technology could become available as early as 1985 for the 1.25 micron feature size IC's. The increased performance of a VHSIC TCS will result in fewer unique designs in support of trainers and therefore shorter design times. VHSIC technology embededed in the design of a core generic training chip (TCS) should be capable of supporting approximately 80% of the processing computation and control requirements of any trainer.

Potential applications of the TCS encompass training requirements for all military services and should be addressed as a future joint service program for insertion. The core TCS has been conceived to support all foreseen applications since it is not platform unique, service unique or limited by performance constraints that could conceivably result in early or premature obsolenscence. The requirements of chip sets for adjunct functions (e.g., visual, ASW simulation, etc.) may be unique. However, in many applications the TCS can support the total real-time processing requirements of some trainers, and thus not require adjunct chip developments.

In summary the VHSIC technology is upon us, its impact is expected to be significant, and its benefits plentiful. VHSIC will impact skills, training concepts as well as trainer devices. It is imperative that we recognize VHSIC's potential, and begin developing plans and techniques for implementing these new concepts.

ABOUT THE AUTHORS

DAVID P. GLENN is currently Director of Research for the Naval Training Equipment Center in Orlando, Florida, and in that capacity is responsible for a training and training device research program in support of multiple Navy platforms. In the past he has served as Assistant Director of the Air Force Simulator SPO and as program manager or research scientist on a number of programs dealing with optics, electro-optics, radar, and telementry systems.

HAROLD T. FREEDMAN is currently Chief Engineer for Advanced Training Programs at Honeywell's Training and Control Systems Operations in West Covina, California. In that capacity Mr. Freedman is responsible for the acquisition and development of new training technology and the infusion of this technology into new training products. In the past, Mr. Freedman has served as Chief Engineer of Training and Control Systems Trainer Systems, responsible for the development of maintenance and operator trainer devices.

DR. JAMES A. GARDNER is currently Manager of Advanced Training Systems Marketing at Operations in West Covina, California, and is responsible for the development of new training systems concepts, technology, and products. In the past, he has served as Marketing Manager, Training Systems Programs, and as Program Manager or research scientist on a number of technology and production programs involving maintenance training, operator training, and video systems.