LSI ADVANCES IN TRAINER TECHNOLOGY

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ABSTRACT

With the capabilities of EW systems and the densities of the EW environment multiplying, the need for large numbers of signal simulators in trainers becomes evident. This puts increasing pressure on the simulator contractors and the procuring agencies to trade off the increased costs of signal densities and realistic training missions. The solution to this problem is increased use of Very Large Scale Integration (VLSI) to produce the basic building blocks needed to create simulated signals.

The number of new VLSI products available to the design engineer today is widely varying and is increasing at an exponential rate. The selection of a VLSI product will dictate the integration capabilities of the design engineer. This paper will describe the process of reducing a board level product to one quarter of its previous space and power requirements.

The selection of a VLSI contractor will dictate the success or failure of the VLSI effort. The claims by various manufacturers can be misleading to the design engineer who normally uses commercial integrated circuits. Once a VLSI contractor is selected the design engineer must construct a breadboard to be used in verification of the computer simulations and also the initial prototype IC's. The simulation tools used by the VLSI contractor and the design engineer aid in the design of the IC and also the probability of the final product working successfully.

The future of VLSI technology in Simulation and Training is virtually untapped and is limited only by the vision of the design engineer. A brief look into where the VLSI manufactuers are heading and how Simulator contractors may capitalize on these trends will be examined.

INTRODUCTION

As the capabilities of today's EW equipment increases, the need for realistic simulation of the battlefield environment in a trainer also increases. This in turn will cause the price of the simulator to increase and the reliability and MTBF to decrease. This puts the responsibility on both the government and the contractor to develop new technologies that will allow increased performance with a minimal effect on cost and reliability. The solution to this problem is the increased use of Very Large Scale Integration (VLSI) to create the building blocks needed for a realistic simulation.

There are a number of technologies available now to the system designer and the selection of the correct technology will determine the success of the product in the marketplace. The commercial products now available are Programmable Logic Arrays, Gate Array logic, Semicustom Standard Cell logic, and Full Custom Integrated circuits. The price for development and low quantity purchases of those products also increase is that order. The use of Programmable Logic Arrays is currently very common and yields only a moderate increase in the packing density and a corresponding decrease in power consumption. While this is the least expensive of the four alternatives it is really only suited for reduction of random logic on the circuit board. The use of Semicustom and Custom Integrated circuits is only economically feasible when a critical space and power requirements are needed or the quantity of devices used is quite large. This leaves the use of Gate Array logic to the simulator system designer.

The selection of the various gate array technologies is heavily dependent upon the requirements of the circuit and the level of integration required. The technologies currently available range from high speed CMOS to bipolar arrays. The CMOS gate arrays currently have the highest speed-power product and also the highest packing density of the available arrays. The designer must thoroughly evaluate the circuit being packaged into a gate array to determine the speed and density required. The division of the circuit into several gate arrays rather than one can lead to a significant decrease in cost of development while having only a minimal impact on the production costs. The system designer must also carefully evaluate the vendors claims of speed and capabilities since these will have a direct impact on the success of the circuit design. Current gate arrays range from 500 to 7000 gates per IC and this density is increasing as the custom IC field becomes more competitive.

Today's system designers are choosing gate arrays for several reasons. The primary reason is to increase the packing density of the simulator and thus increase the price/performance ratio of the system. A secondary reason is to allow the designer to increase the processing speed of the simulator beyond that which is possible with discrete logic. The process by which the designer chooses the circuit to be placed into gate arrays is wildly varying but must follow a few basic rules. The first constraint is the quantity of IC which will be used by the company over the life of the product. The cost of the IC development is directly related to its complexity and the quantity of the IC being used in the near future. Gate Array manufacturers generally tie the development cost of the IC to the quantity they expect to be purchased in the near future. Thus, the selection of a circuit for gate array development must have sufficient quantity to justify the cost of development and production.

The second constraint placed on the gate array designer is the speed at which the circuit

must operate. Currently available CMOS arrays have gate delays in the 5 nanosecond range while the newer gate arrays have dipslays in the 2 ns range. As the arrays become more dense the speed at which they operate also increases. The penalty for this is that as the technology becomes more complex the probability of problems surfacing in test increases. This increases both the development time, costs for development, and also increases testing time and cost for each IC. Both of these items must be at the forefront when deciding what circuits to place into gate arrays.

AAI is currently producing several gate array circuits to be used in their EW simulators and System Test equipment. These circuits were selected for gate arrays for several reasons. First the quantity which would be produced would be sufficiently high and the manufacturing cost of discrete logic boards would justify the cost of the gate array development and production. A second major reason for one of the gate arrays is the decrease in power consumption and size of the total system. A third major reason is the cost of the supporting hardware required, such as power supplies, card racks, etc.

A Programmable Pulse Generator (PPG) was one of the gate arrays developed by AAI. The major reasons that this circuit was selected for gate array development were the following:

1) high cost of the currently manufactured PPG board

2) space requirements of newer trainers due to increased signal densities

3) power consumption due to increased signal densities

The development of the PPG gate array will be traced from its initial conception to a working prototype (see Figure 1).

EXAMPLE

The PPG board is a programmable radar pulse train generator which has been used on the B-52, A-10, and other AAI EW simulation programs. The PPG is a fully programmable special purpose microprocessor whose instruction set has been chosen specifically for the reproduction of radar pulse trains. The PPG board was originally developed using Schottky TTL, contained 54 IC's, and required 2.2 amperes of 5 volt power. Each PPG board was 6 inches by 9 inches and would produce one radar pulse train. Since typical signal densities on EW simulators range from 64 to 300 signals the quantity of PPG's required ranged from 32 to 200. This quantity of PPG boards consumed large amounts of power and space in the simulator and AAI felt to remain competitive that a newer PPG must be developed. A goal was set to produce a PPG which would put 4 radar pulse train generators on the same size board consuming the same power as the original PPG.

The PPG contains a micro-sequencer, RAM, PROM, and several high speed counter which acts as a single processor. The circuit operates at 10 MHz and can generate pulse trains of 100 nanosecond resolution. The first step in the gate array design was to partition the circuit into items that could easily be put in a gate array. After some analysis it was determined that the RAM and support circuitry for I/O would be common for all PPG gate arrays on the board and that the counters and microsequencer would be put into a gate array. The four PPG gate arrays would share the common RAM and the result would be a board which produced 4 pulse trains. Since this design was different from the original PPG board in design a prototype PPG board was constructed from conventional TTL logic and tested. This prototype was tested with new test programs which took advantage of several added features along with older programs to insure compatability. Once the prototype was thoroughly tested a final schematic of the gate array was produced using conventional TTL logic symbols, an initial set of test vectors, and a device specification was written.

The selection of a gate array company turned out to be a major undertaking consuming many hours of evaluation. Claims of 20 to 30 MHz toggle rates by many companies turned out to be only in special cases and they could not meet the 10 MHz throughput rate of the PPG. It was determined that the PPG IC required about 3800 gates and the typical gate delay would have to be in the 2-5 ns range. After evaluating many manufacturers and their devices it was determined that LSI Logic and their 5000 series gate array was the only device then available that could meet these requirements. This series used 3 micron gates, had a maximum of 5000 gates in a chip, and had a typical gate delay of 2.5 ns with a maximum gate delay of 5 ns. LSI Logic had also developed a development station capable of supporting the gate array development from start to finish with a maximum of computer aided engineering. This would lead to a timely development of the chip with the lowest cost and highest probability of success.

LSI Logic allows a customer two methods of developing a gate array circuit. The first method, which is perferred by LSI, is that the customer send an engineer to LSI for training. The engineer with assistance from a LSI applications engineer would then take his gate array and enter it into the computer for simulation. This is the desired method since it allows the customer to learn more about gate array development and spread that knowledge throughout the company. The second method, which was used to develop the PPG, is to send LSI a schematic and have their applications engineer totally develop the IC. This is more expensive than the first method since the LSI engineer must first learn how the circuit works before he can generate the required data. This method was chosen, however, due to the short development time required for the PPG.

The first step of the IC development is to take the schematic and enter it into LSI's computer system for simulation. This task can be difficult or easy depending upon the companies library of TTL equivalent gate array macros. LSI Logic has a complete set of these equivalent macros and this entry went very quickly. One problem with the TTL macros is that all of the gates in the macro may not be required by the circuit. A "gate eater" program solves this

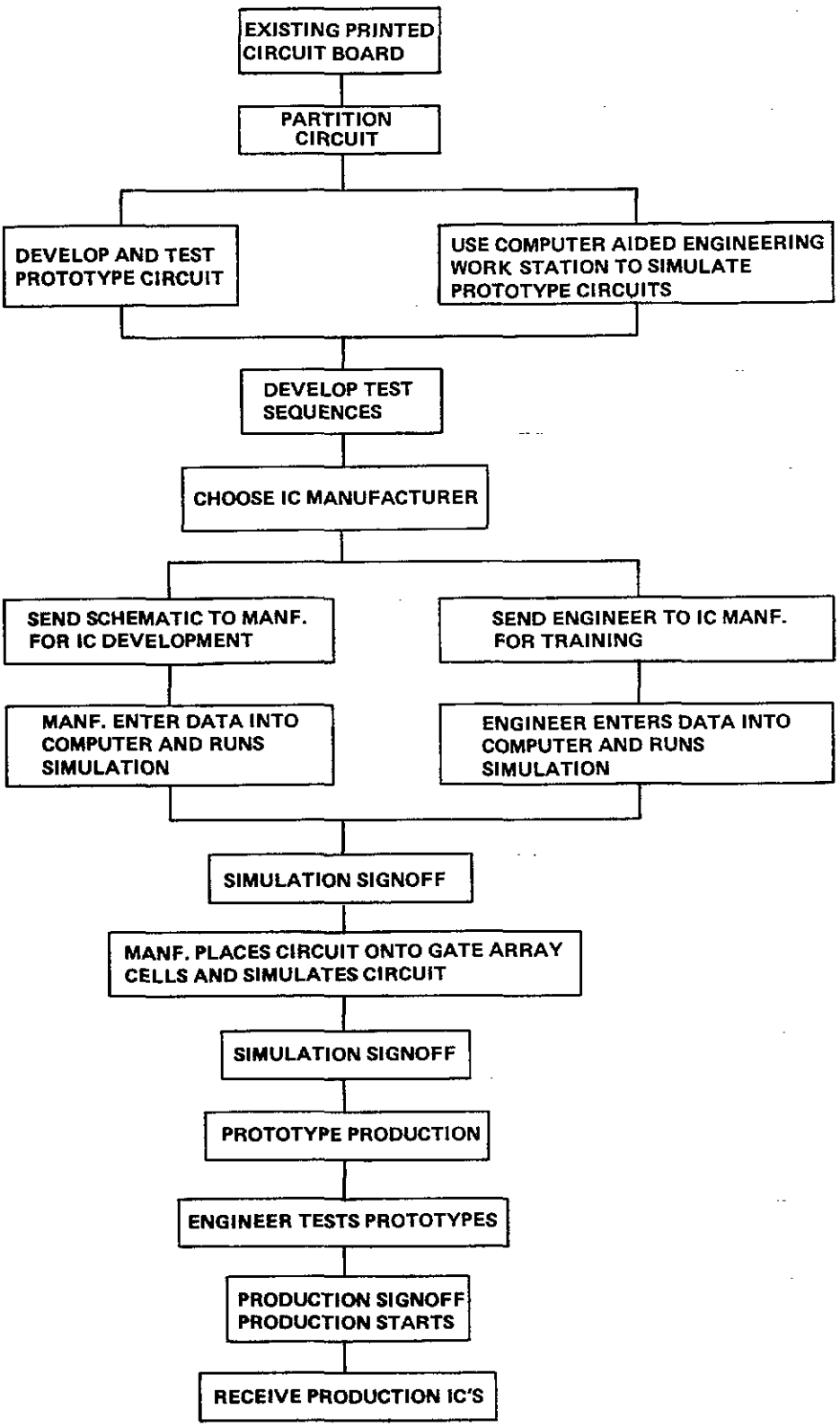
EXISTING PRINTED CIRCUIT BOARD
PARTITION CIRCUIT
DEVELOP AND TEST PROTOTYPE CIRCUIT
USE COMPUTER AIDED ENGINEERING WORK STATION TO SIMULATE PROTOTYPE CIRCUITS
DEVELOP TEST SEQUENCES
CHOOSE IC MANUFACTURER
SEND SCHEMATIC TO MANF. FOR IC DEVELOPMENT
SEND ENGINEER TO IC MANF. FOR TRAINING
MANF. ENTER DATA INTO COMPUTER AND RUNS SIMULATION
ENGINEER ENTERS DATA INTO COMPUTER AND RUNS SIMULATION
SIMULATION SIGNOFF
MANF. PLACES CIRCUIT ONTO GATE ARRAY CELLS AND SIMULATES CIRCUIT
SIMULATION SIGNOFF
PROTOTYPE PRODUCTION
ENGINEER TESTS PROTOTYPES
PRODUCTION SIGNOFF PRODUCTION STARTS
RECEIVE PRODUCTION IC'S

FIGURE 1

problem by purging the input circuit of all unused gates. At this time a logic simulation was run on the PPG to verify correct operation of the IC. This simulation was reviewed by the AAI engineer responsible for the PPG and after several tests was approved for prototype development. At this point the remainder of the IC development was LSI's responsibility since it involved only gate layout and interconnect.

LSI's workstation allowed rapid computer aided layout of the PPG circuit. As a design rule only about 80% of the gates on the IC should be used since the layout time increases as the utilization increases. Computer aided design rule checking and fault detection analysis also help insure the success of the PPG development. Once the PPG was laid out on the gate array a final simulation was done to incorporate the delays due to wire lengths inside the IC. The simulation results and test vector tape was reviewed by both LSI and the engineer at AAI and approved. This final check gives LSI the approval to produce several prototype IC's.

Once the prototype IC's are produced they are tested by LSI using the test vectors from the simulation. Once the samples are tested by LSI they are then shipped to AAI for testing in the actual circuit. At AAI the IC's were placed in the prototype circuit board and tested. Once testing is completed by both LSI and AAI the approval is given for production of PPG IC's.

As engineers increase their use of custom IC's there is a large amount of education required in the field of IC testability. While it is very easy for an engineer to probe a circuit board under development or use bed of nail testers on production boards, it is very difficult to test the internal workings of an IC. These new testing requirements come as a shock to the design engineer and some of the techniques used for IC testing are totally unfamiliar to the *circuit board designer. For example, LSSD* testing which is easily used on IC's is next to impossible to implement on a typical circuit board. The designer should remember that a 10-20% increase in the number of gates used for testing will not decrease the reliability of the circuit but will decrease the test time required for the completed IC making it cheaper to manufacture. Several of the newer gate arrays incorporate test circuits into their gate arrays as standard circuits which may not be removed, thus showing the IC companies commitment to gate array testability.

CONCLUSIONS

The future of custom IC development looks very bright for companies of all sizes. The number of custom IC companies is increasing monthly and the competition is pushing the development of densier arrays and advanced development software. A number of companies are now developing desktop engineering workstations capable of gate array development at a low cost. With more companies in the gate array field the cost of gate arrays will decrease dramatically. Also gate arrays are increasing in speed and density allowing systems which previously required ECL logic to be done in CMOS gate arrays. Several companies are now offering full custom IC development at a reasonable cost. These new IC's will be more complex than gate arrays and consume less power for the function performed. Several workstation companies are currently working on a software to allow full custom logic development on their systems thus lowering costs even more.

The use of custom IC's has now come within reach of many companies building simulators and their increased use will allow them to become more competitive. But this new capability is not without its price to the company wishing to take advantage of it. The education of their engineers in the techniques of VLSI design and testing should be of primary concern before undertaking any in house IC development. With the knowledge of IC design techniques simulation companies taking advantage of custom IC's will improve their position in today's competitive market.

ABOUT THE AUTHOR

MR. THOMAS BACHMAN is a design engineer with AAI Corporation in Cockeysville, MD. He is currently a lead engineer responsible for EW simulation on the EF-111A OFT. He formally worked as a design engineer on several EW simulators including NEWTS and B-52 WST. He holds a Bachelors degree from University of Delaware in Physics and has been with AAI Corporation six years.