

# ULTRA-HIGH RESOLUTION DMT VISUAL DISPLAY VIA PC-IG ARRAY TECHNOLOGIES

Ben L. Surber

L3 Communications, Link Simulation & Training Division  
Mesa, Arizona

Dutch Guckenberger, PhD  
SDS International, Inc.  
Orlando, Florida

## ABSTRACT

The Air Force Research Laboratory/Warfighter Training Research Division (AFRL/HEA) located in Mesa, Arizona, has been developing Ultra-High-Resolution (UHR) projector technology since the mid 1990's. A major lab goal is to provide Air Force fighter pilots with eye-limited resolution during their simulator training scenarios. Based upon display geometry of the Boeing Visual Integrated Display System (VIDS) and the Air Force's Mobile Modular Display for Advanced Research and Training (M2DART), a UHR projector capable of displaying an unprecedented resolution of 5,120 pixels by 4,096 lines at 60 Hz frame rate is required. The Air Force has several such UHR concepts in development. A UHR projector meeting these requirements would have a bandwidth of 1.3 giga pixels per second. This pixel bandwidth is an order of magnitude higher than what any single channel Image Generator (IG) currently produces. One way to achieve such bandwidths is to use multiple IG channels in parallel.

PC based IG capabilities have been increasing at a rapid rate and are relatively inexpensive compared to their mainframe IG predecessors. This makes PC-IGs the most likely selection to drive the UHR displays of the future. However, depending upon the application, PC-IGs can have some significant trade-off differences vs. the mainframe IGs. Historically, when a single PC-IG channel is used to drive large fields of view in fixed-wing aircraft training simulations, they demonstrate a lower database retrieval range than mainframe IGs, which can result in restrictions being placed on the pilot's visibility range. Current Digital Visual Interface (DVI) compliant graphics adapters used in PC-IGs only support up to HDTV video formats.

The authors posit that PC based IG performance limitations can be overcome with an innovative approach to combine digital video outputs from synchronized PC-IG arrays. Since each PC-IG of the array only processes a small segment of the UHR display's field of view, the supportable scene complexity could be dramatically increased at a performance level exceeding that of mainframe IGs. This paper explores the architectural design concepts and associated technologies of driving UHR visual displays by combining digital video outputs from synchronized PC-IG arrays.

## ABOUT THE AUTHORS

Ben Surber graduated from DeVry Institute of Technology in September 1976. He holds a Senior Systems Engineering position with Link Simulation & Training Division of L-3 Communications Corporation where he has been employed for 22 years. He has been assigned to the Air Force Research Laboratory AFRL/HEA facility in Mesa, Arizona for over 12 years. He is part of a team dedicated to advancing the development of ultra high-resolution displays and the image generation systems that drive them.

Dr. Dutch Guckenberger is the Chief Scientist at SDS International, with 16 years of experience in defense simulation and training systems. He has earned degrees in Computer Science, Physics, & Simulation and Training. Research interests include Distributed Mission Training, High Resolution PC-Based Visual Systems, Appended Training Systems, Above Real-Time Training (ARTT), UAV and UCAV Research. He is a member of ACM, IEEE, SPMN, Human Factors Society and a Link Foundation Fellow in Advanced Simulation and Training.

# ULTRA-HIGH RESOLUTION DMT VISUAL DISPLAY VIA PC-IG ARRAY TECHNOLOGIES

Ben L. Surber

L3 Communications, Link Simulation & Training Division  
Mesa, Arizona

Dutch Guckenberger, PhD  
SDS International, Inc.  
Orlando, Florida

## INTRODUCTION

Air Force fighter pilots require eye-limited resolution for many simulator training scenarios and tasks. To provide eye-limited or 20/20 visual acuity in a Boeing-St.Louis Visual Integrated Display System (VIDS) and the Air Force's Mobile Modular Display for Advanced Research and Training (M2DART), a ultra high resolution (UHR) projector capable of displaying an unprecedented resolution of 5,120 pixels by 4,096 lines at 60 Hz frame rate is required. The Air Force Research Laboratory (AFRL) is supporting several UHR concepts designed to meet this order-of-magnitude performance increase. Some projector manufacturers are indicating that they will meet the demanding challenge of presenting 5,120 x 4,096 pixels from a single projector.

An affordable image generator capable of driving a UHR projector with high detail scene content is of paramount importance. Indications are that combining multiple digital video outputs from independent PC-based image generators (PC-IGs) could be a viable solution. This paper explores the architectural design concepts and associated technologies of driving a UHR visual display by combining digital video outputs from synchronized PC-IG arrays. Two possible architectures that could be used to build a PC-IG Digital Video Combiner (DVC) outputting UHR resolution imagery will be presented. The DVC device as discussed in this paper is an independent system that interfaces between multiple synchronized PC-IG channels and a UHR projector. However, it is anticipated that the DVC functionality could and eventually will be incorporated within some UHR projectors.

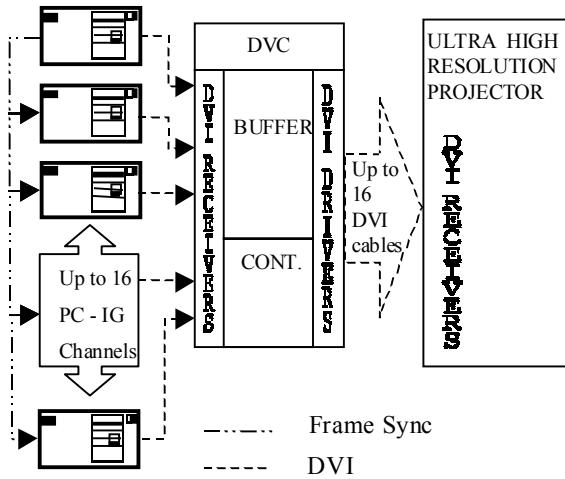
## TWO POSSIBLE ARCHITECTURES FOR A DIGITAL VIDEO COMBINER (DVC)

The first architecture to be described uses commonly available video formats as inputs and outputs a combined tiled format. The second architecture presented uses presently unavailable and unconventional video formats as inputs and outputs a combined striped format. This striped output would be most advantageous when used to drive spatial light modulators that are capable of painting one entire line of video as soon as the line is received. To help clarify, modulators that can update lines at the line rate as opposed to the frame rate. Both architectures have the following in common:

- Eliminate blending issues normally associated with analog video combining techniques.
- Could enable dramatic increases in scene complexity to levels exceeding that of mainframe IGs. This is an extremely significant advantage because it even applies to displays having conventional resolution capabilities.
- Allow for timing differences that can result from acceptable tolerances between independent PC-IGs, only requiring that their update rate and video outputs are frame locked.
- Video inputs must be in compliance with the Digital Visual Interface (DVI) specification. In addition, the video format being output from the independent PC/IG channels must be of the same resolution and be non-interlaced.
- Use each independent PC-IG channel's recovered DVI clock to write data into the DVC's buffers.

- Use a common clock to output data via DVI to the UHR projector.

Figure 1 shows a block diagram, that applies to both architectures, using sixteen independent PC-IG channels to drive a UHR projector via a DVC. The fundamental deference of the two architectures resides within the DVC's video buffer and will be described later.



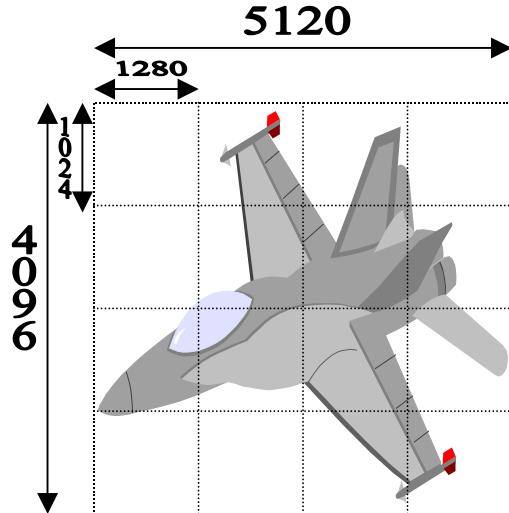
**Figure 1. Hardware Block Diagram for Both Approaches.**

In the following description of the tiled architecture approach the sixteen PC - IGs are outputting a commonly supported progressively scanned video format of 1280 x 1024 @ 60 HZ. The sixteen PC - IG video outputs are frame synchronized and each output fills a specified section of the double buffered frame buffer within the DVC. These frame buffers need to be large enough to support the desired DVC output resolution at 12 bits per color. For the UHR projector of the resolution described here this equates to  $5120 \times 4096 \times 36 = 755$  megabits or 95 megabytes per buffer.

As stated previously, the DVC uses each independent PC - IG channel's recovered DVI clock to write information into specified memory locations. The significance of using each independent channel's recovered DVI clock, to write that channel's information into a common frame buffer, is that it enables the incoming video to only be frame locked instead of pixel locked.

While one of the DVC frame buffers is being filled the other frame buffer is being read (one scanline at a time) using a common clock, and is output via

the DVC DVI drivers to the UHR projector. Figure 2 shows a representation of this tiled video output, each square being the area one PC - IG would have produced and sent to the DVC frame buffer.



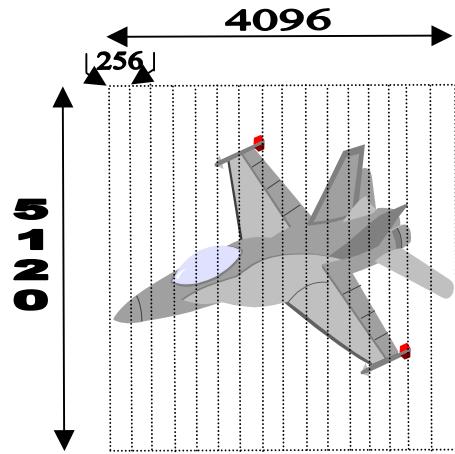
**Figure 2. Tiled Sixteen 1280 x 1024 Formats.**

Each video channel of the PC - IGs used to support this illustrated concept, would have a DVI operating at 80 million pixels per second. At the 60 HZ frame rate, the DVI specification supports a 165-million pixel bandwidth in single link mode and 330-million pixel bandwidth in dual link mode. This means that the number of PC - IG video channels could be potentially reduced to 8 in single link mode and 4 in dual link mode drastically reducing associated PC-IG cost. Of course, this potential reduction could only be achieved once each PC -IG video channel can produce these bandwidths.

Unfortunately, this tiled frame buffer architecture will contribute an additional frame time of throughput delay. For fixed wing aircraft simulations, this additional lag time may be unacceptable, especially if the projector technology being utilized already consumes a frame time over the conventional CRT based displays. However, if the projector technology being utilized can support the parallel pixel writing of one dimension's worth of the video format being displayed then the throughput lag time can be significantly reduced.

Figure 3 shows a striped buffer architecture. In this illustration, each of the sixteen IG channels would be responsible for supplying a long vertical stripe of video. Each stripe would be 256 pixels wide and

5120 scanlines long. There are two reasons behind this architecture. First, it has the potential of reducing the DVC throughput delay to only a few scanlines. Second, it can also greatly reduce the size of the video buffer internal to the DVC. The minimized throughput delay would be the consequence of the striped architecture and being able to read from the first part of the buffer while the remaining buffer area is still being filled. In this approach, each of the frame synchronized DVI inputs would be allowed to write into its own area of the video buffer utilizing its own DVI clock. After the first part of the buffer is filled with several scanlines, the DVC starts outputting the first lines of video (using a common clock) to the projector, while the remaining buffer area is still being filled. The vertical blanking is made long enough to compensate for any differences in individual IG channels frame completion times. The frame sync is not sent to the IG channels until after all the channels have completed their frame.



**Figure 3. Striped Sixteen 256 x 5120 Format.**

The benefit of greatly reducing the size of the DVC's internal video buffer would be accomplished by using a rolling scanline buffer technique. In the following discussion the DVC's scanline buffer is 4096 pixels wide and 12 lines deep. The depth of 12 scanlines was arbitrarily chosen. In reality the depth just needs to be sufficient to allow for compensation of incoming video timing differences and control circuits within the DVC. The scanline buffer memory size would be  $4096 \times 36 \times 12 = 1.77$  Megabits or 222 Kilobytes.

Initially the first 4 scanlines of an incoming frame of video are written into scanline buffer addresses 1 through 4 (see Table 1).

Scanline number of the data being written, by each individual PC-IG, to the DVC buffer.	DVC Write Buffer Address	DVC Read Buffer Address	Scanline number of the data being output from the DVC to the projector input.
SL=1	1		
SL=2	2		
SL=3	3		
SL=4	4		
SL=5	5	1	SL=1
SL=6	6	2	SL=2
SL=7	7	3	SL=3
SL=8	8	4	SL=4
SL=9	9	5	SL=5
SL=10	10	6	SL=6
SL=11	11	7	SL=7
SL=12	12	8	SL=8
SL=13	1	9	SL=9
SL=14	2	10	SL=10
SL=15	3	11	SL=11
SL=16	4	12	SL=12
SL=17	5	1	SL=13
SL=18	6	2	SL=14
SL=19	7	3	SL=15
SL=20	8	4	SL=16
SL=21	9	5	SL=17
SL=22	10	6	SL=18
SL=23	11	7	SL=19
SL=24	12	8	SL=20
SL=25	1	9	SL=21
SL=26	2	10	SL=22
SL=27	3	11	SL=23
SL=28	4	12	SL=24
SL=29	5	1	SL=25
Etc. Until end of active scanlines	Etc. Until end of active scanlines	Etc. Until end of active scanlines	Etc. Until end of active scanlines

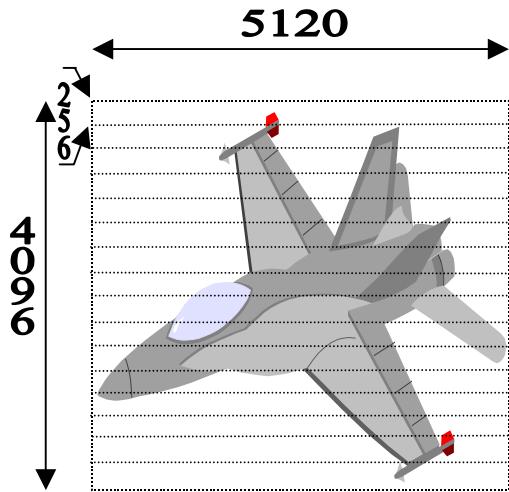
**Table 1. Rolling Scanline Buffer Technique.**

As incoming scanline video for scanlines 5 through 8 is being written one line at a time into buffer address 5 through 8, the buffer read has begun on address 1 through 4. As incoming scanline video for scanlines 9 through 12 is being written one line at a time into buffer address 9 through 12, the buffer read has begun on address 5 through 8. As incoming scanline video for scanlines 13 through 16 is being written one line at a time into buffer address 1 through 4, the buffer read has begun on address 9 through 12. As Table 1 indicates, this cycling or rolling of the buffers continues until all

the scanlines within the frame have been processed.

The striped approach has the same potential reduction in the number of PC - IG video channels that the tiled approach has, down to 8 in single link mode, and 4 in dual link mode.

Figure 4 shows the striped format in the more conventional  $5 \times 4$  aspect ratio. It is produced in the same way, and has the same advantages, as that of Figure 3. In fact, it is accomplished by doing nothing more than rotating the projector 90 degrees, and instructing each IG channel to roll its perspective correspondingly by 90 degrees. This can cause some confusion, because what is normally considered to be each IG channels horizontal pixels, are now being displayed vertically and vice versa.



**Figure 4. Striped Approach Shown with a Conventional  $5 \times 4$  Aspect Ratio.**

Hopefully graphics adapter manufacturers will soon recognize the benefits of striped video formats for UHR projectors. Until manufacturers allow users to define such formats advantages of minimal throughput lag and small buffer size cannot be realized.

#### ADDITIONAL ABILITIES

The ability to dramatically increase scene complexity was previously described as one of the possible benefits of multiple PC-IGs computing independent sections of a UHR projector's field of view. The additional scene complexity that can be achieved will be related to how well the associated software and terrain databases are optimized for

the selected graphics adapter's abilities. This potential benefit would not be restricted to UHR displays. There are many applications desiring to increase the scene complexity of displays with substantially lower than UHR. The DVC approach could allow current day displays to be driven at their maximum resolution and significantly improve the amount of scene content.

While the following additional features are considered beyond the scope of this paper, and will not be described in detail, they are mentioned to show the extreme versatility that can be incorporated within a DVC.

The DVC concept is not limited to being driven by PC-IGs, any IG capable of meeting the input requirements could be used.

An additional cost-reducing feature could be added to enable UHR displays to be driven with less than the maximum number of IG channels. This could be accomplished by incorporating input scaling capabilities that allow up sampling of the inputs while they are written to the DVC's video buffer.

Should the user decide to implement the up-sampling technique, a target inset feature could also be incorporated. This could allow multiple alpha blended targets to be shown at the ultra high resolution even though the remaining scene is being up-sampled at a lower resolution.

#### DVC FORMATS

The DVC described above would be capable of supplying over 1.3 giga pixels of video per second. As many as sixteen single link DVIs were described operating in parallel to input and output the digital video. Each single DVI link could potentially support a 165 million pixels per second. It is anticipated that future versions of the DVC would use dual link DVIs that support up to 350 million pixels per second. The DVC architecture is extremely scaleable due to the parallel nature of design.

#### CONCLUSIONS

AFRL in cooperation with industry partners is developing UHR projectors with greater than  $5K \times 4K$ , 60HZ, non-interlaced resolution. Affordable imagery to drive these projectors will be needed. Using large mainframe computers to supply these demanding capabilities will most likely be too

expensive for most military applications. Using multiple PC graphics channels to drive a UHR projector via a DVC has many benefits and can make the imagery affordable. There are two approaches, one that uses commonly available video formats and one that uses unavailable and unconventional video formats. If PC graphics card manufacturers will support these unconventional video formats, then both the video buffer size and the throughput lag time can be drastically reduced. Additional cost saving features could be added within the DVC to allow up sampled background video with ultra high-resolution alpha blended target insets. If needed, this could allow for the use of legacy image generation systems already in place.

## **REFERENCES**

Digital Visual Interface (DVI) Specification, Revision 1.0 April 1999, Published by the Digital Display Working Group (DDWG).